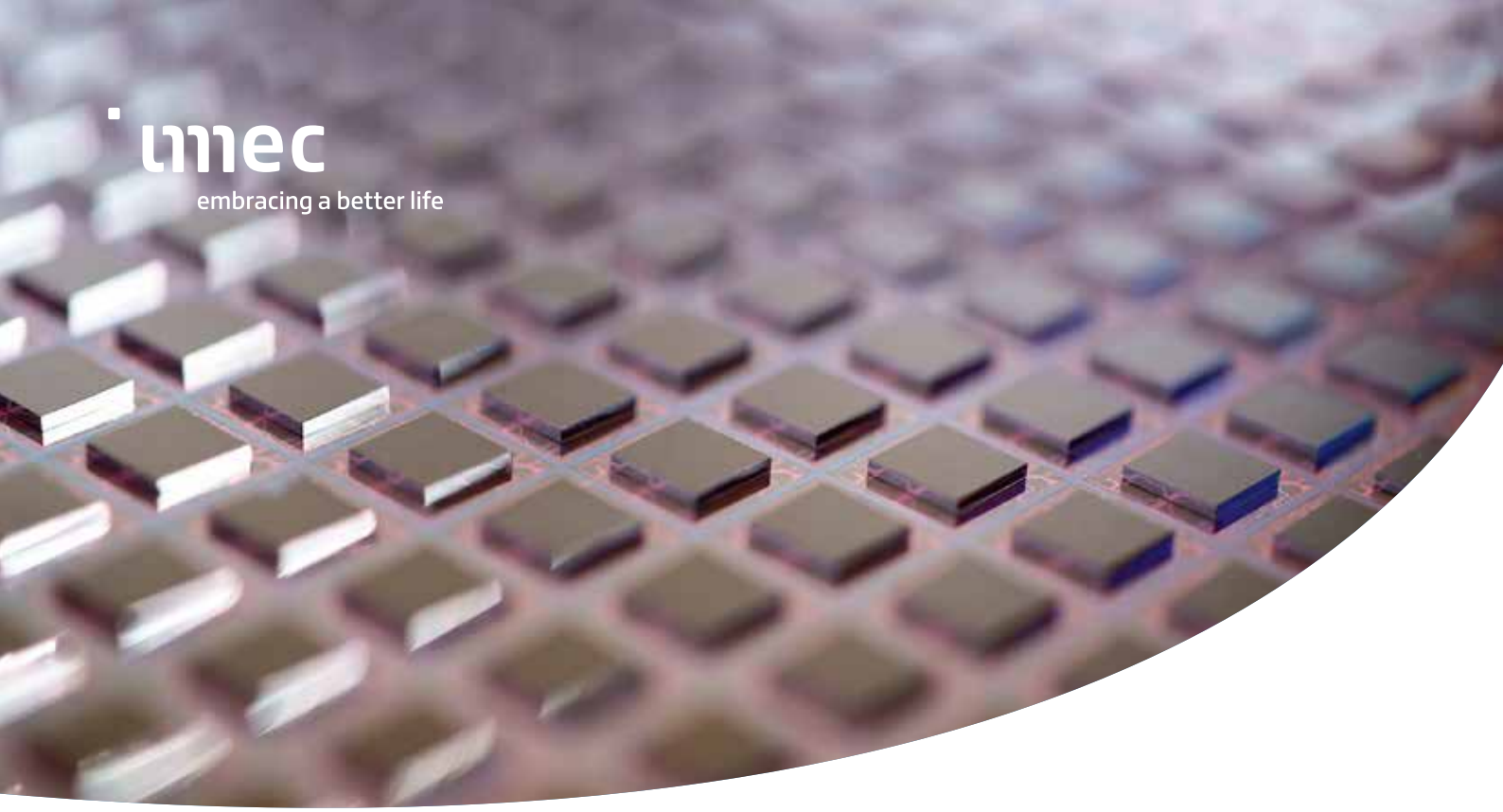


SMART INDUSTRIES

SMALLER SRAM MEMORY FOR FUTURE CHIPS

SRAM, an acronym for Static Random-Access Memory, is a fast and volatile memory used on computer chips. The basic memory element is the SRAM cell, which can store one bit. Today's SRAM cells are made with six transistors. Imec is looking to make smaller SRAM cells to drive future generations of chips. This demo shows two types of advanced SRAM cells based on complementary FETs and surrounding-gate nanowire transistors respectively.

FAST MEMORY CELLS

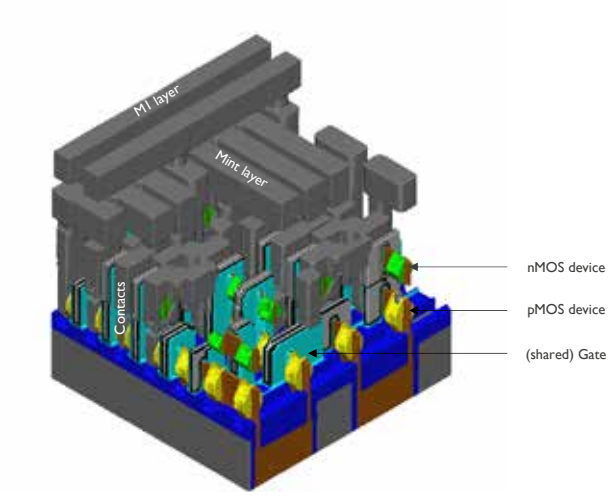
Imec is continuously in pursuit of developing technologies that help build ever more powerful chips with ever smaller components. Our scientists are looking to make transistors – the basic building blocks of chips – smaller and more efficient. They do so by trying out new materials and new transistor geometries. With these new transistors they build basic circuits, such as SRAM memory cells, which they also try to make faster and more energy efficient. SRAM memory cells are not the smallest form of memory to store a bit. SRAMs are made of six transistors whereas DRAM (Dynamic Random-Access Memory) uses only one transistor and a capacitor, and thus can be made smaller and cheaper. But SRAM is faster, requires no refresh, and uses less power. So whenever speed is key, SRAM is used. That is the case for the highest levels of cache memory on a chip, the memory that stores the parameters and data that need to be accessed most urgently by the processor.

TWO NEW DESIGNS

To make SRAM cells smaller and more efficient, imec's scientists explore innovative ways to accomplish the same functionality – storing one bit – in a smaller footprint while at the same time consuming less energy.

The first design developed by imec researchers is based on complementary FET transistors, a concept pioneered by imec that uses vertically stacked complementary transistors. In a typical SRAM layout, the n-type or p-type transistors are fabricated next to each other, in complementary FET (CFET) the two complementary types of transistors used, n and p, are stacked on top of each other. Our analysis shows that this configuration may reduce the area of SRAM cells by as much as 50%.

3D model of SGT SRAM cell.



3D mode of CFET SRAM cell.

The second innovative architecture is the result of a joint project with Unisantis Electronics. It makes use of surrounding-gate-transistors (SGT), which were invented and proposed by Dr. Fujio Masuoka. In these transistors, the gate is fully wrapped around the thin conduction channel (the nanowire) of the transistor, instead of only contacting part of it. This allows a better electrical behavior, which in its turn makes it possible to design smaller transistors, and thus also smaller SRAM cells. For example, using similar technology and dimensions to those involved in the 14nm node one can build an SGT SRAM cell with a 3x smaller area and that uses 50% less energy.

TWO GENERATIONS AHEAD

Both these innovative designs are proposals for future chips, at least two technology generations (approximately three years) in the future. They outperform today's SRAM cells made using FinFET transistors, but they could be fabricated reusing much of the existing fabrication process involved in making FinFET transistors, giving them a higher likelihood of being adopted as preferred solution.

Imec's work on scaled devices is embedded in an open innovation R&D platform that involves the entire value chain of the semiconductor industry, from tool and material suppliers to IDMs and foundries, fabless & fablite companies and system and application partners. The SGT SRAM demonstration is sponsored by Unisantis electronics.

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