2019 VLSI TECHNOLOGY SYMPOSIUM KYOTO

2019 VLSI CIRCUITS SYMPOSIUM KYOTO

12-EUV Layer Surrounding Gate Transistor (SGT) for Vertical 6-T SRAM: 5-nm-class Technology for Ultra-Density Logic Devices

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Outline

- Motivation
- SGT 6-T SRAM Key Design & SRAM Equivalent Circuit
- SGT SRAM Process Steps & Process Optimization
  - FEOL
  - MOL / BEOL
- Device Characterization
- Summary & Outlook

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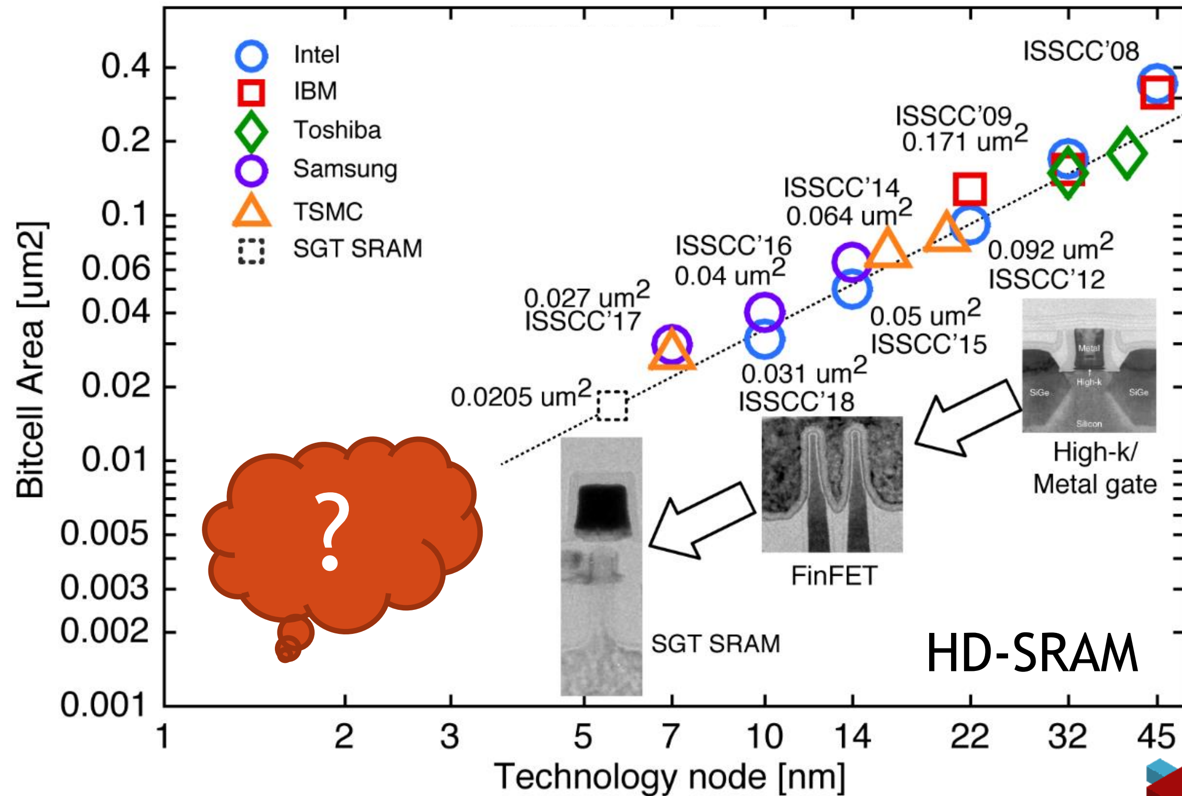
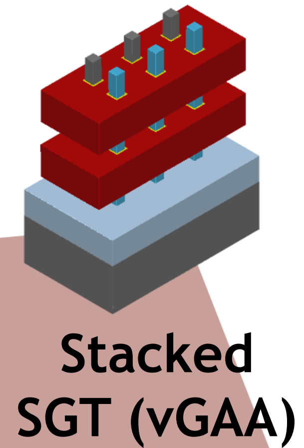
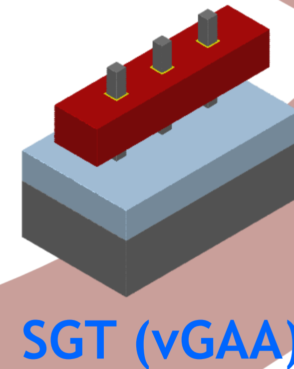
Why Vertical Integration for Future High-Density SRAM?

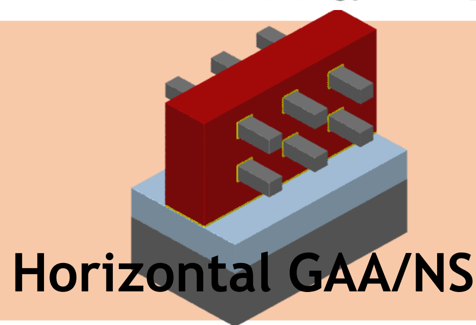




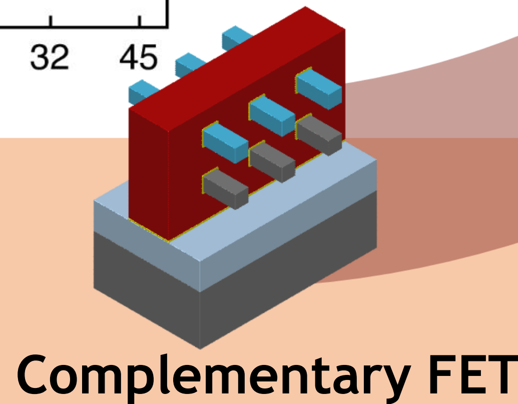
Stacked SGT (vGAA)



SGT (vGAA)

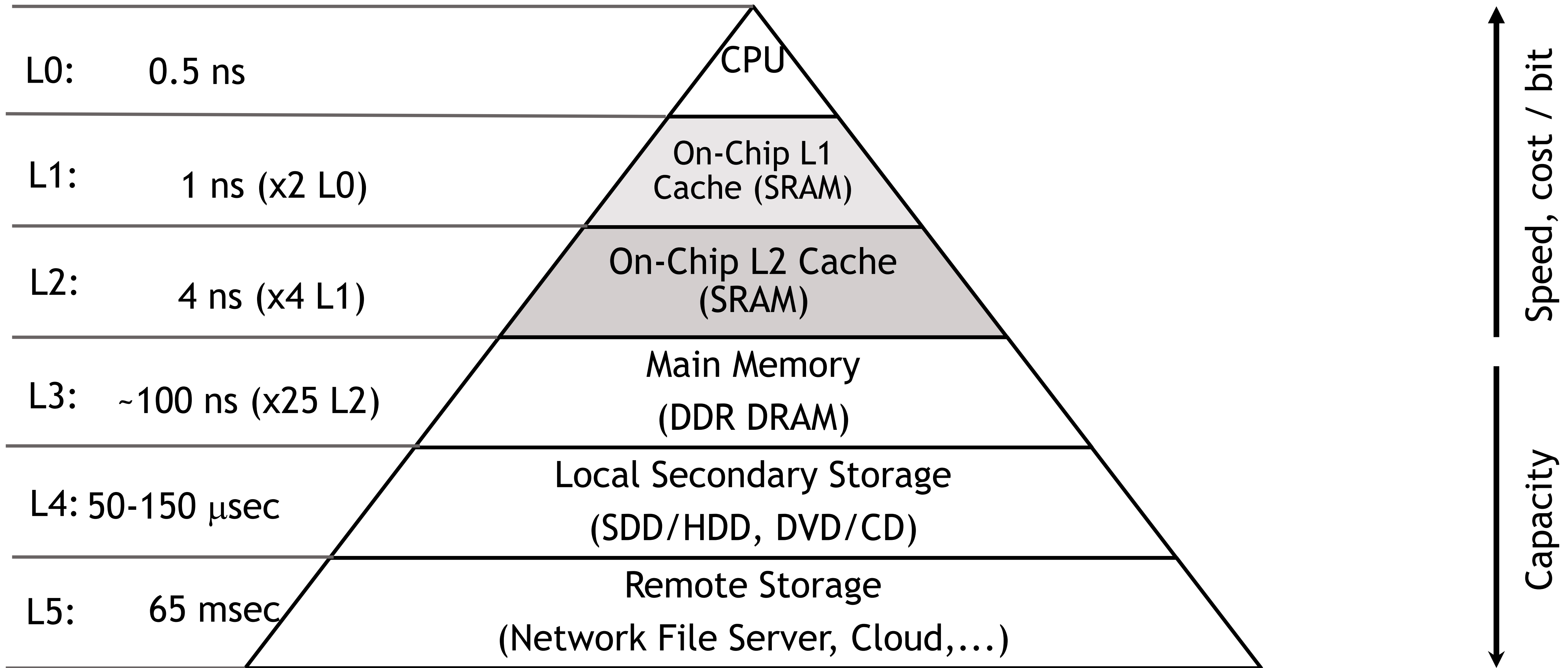


Horizontal GAA/NS



Complementary FET

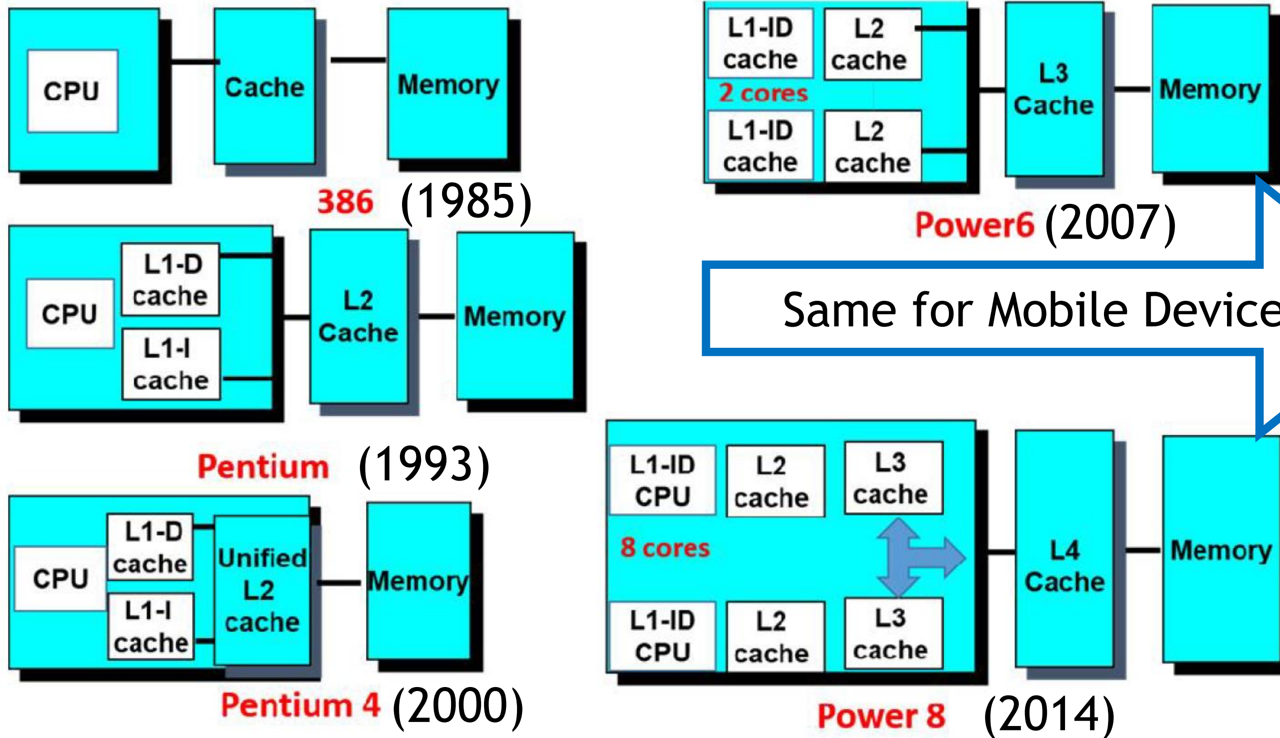
Memory Hierarchy of Computing Device and Lx Cache



[After Andrei Pavlov, 2008 & Intel]

High big Lx Cache is enough?

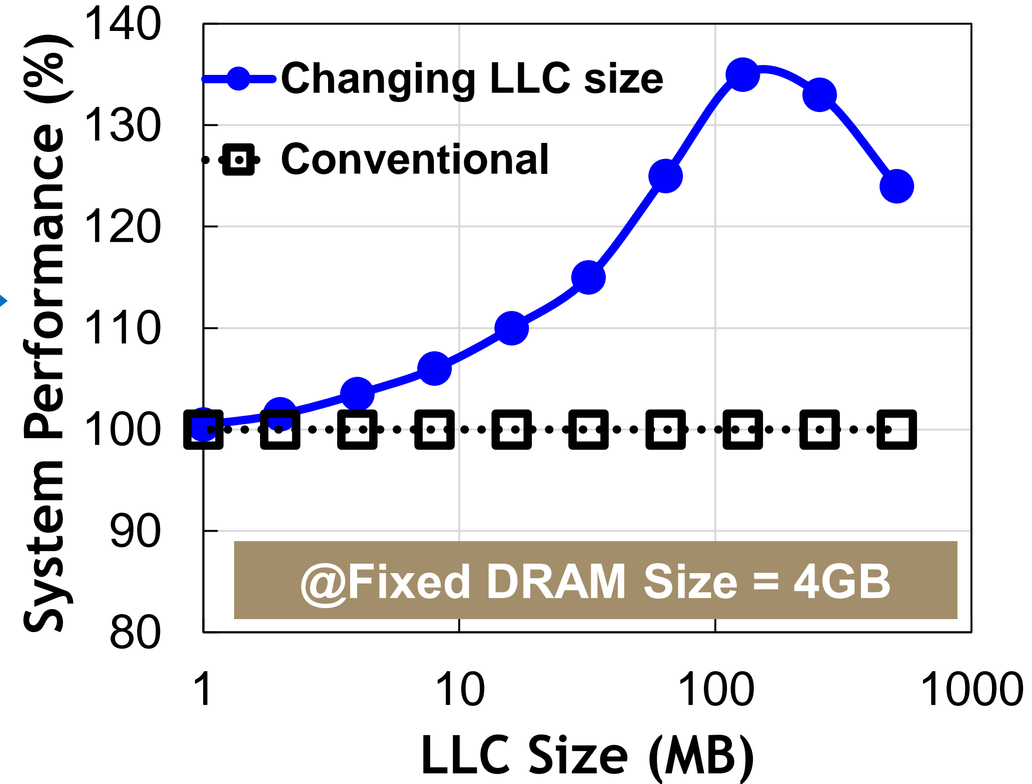
+1 level of cache introduced every ~7 years



[Dl. Etiemble, “45-year CPU evolution: one law and two equations”, 2018]

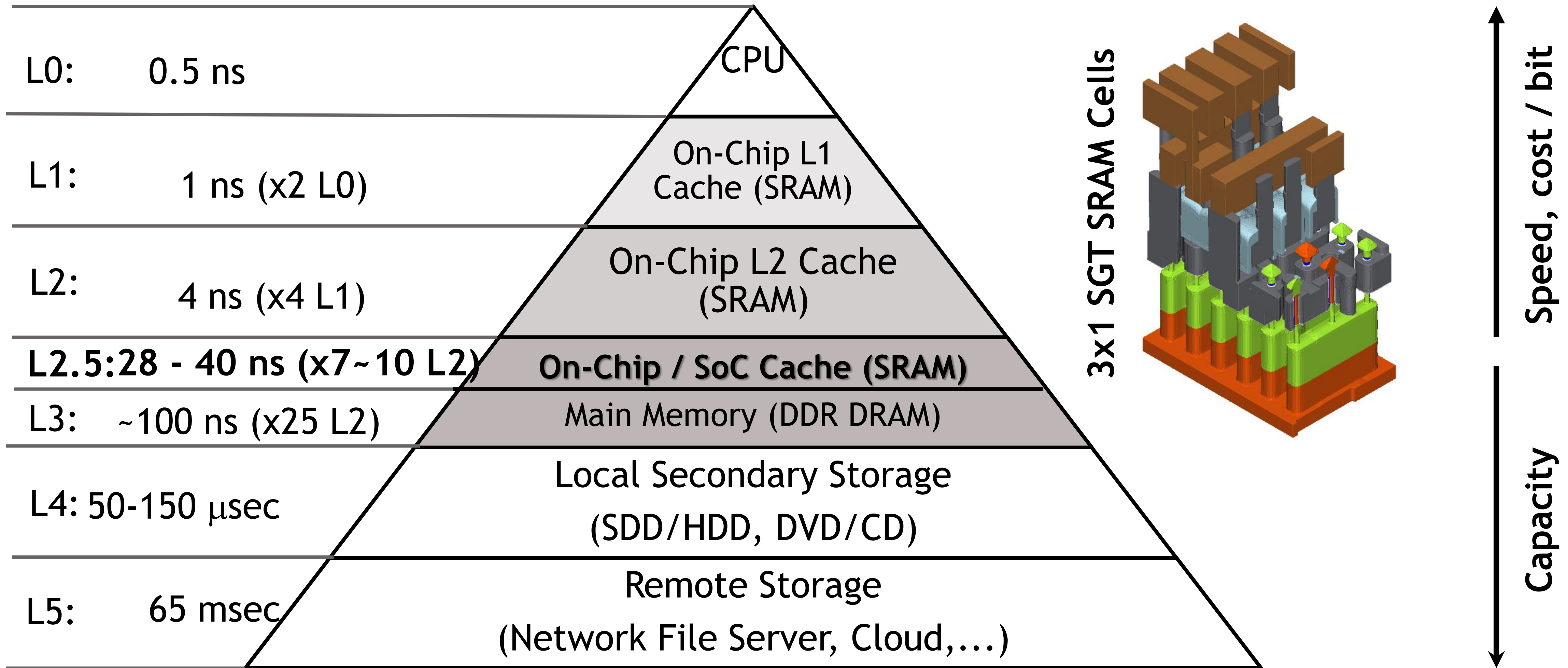
[T. Huynh-Bao, to be published]

ARM Big.Little architecture simulation



- A 128 MB last level cache (LLC) is shown to be optimal from the gem5 simulation

Memory Hierarchy of Computing Device and Lx Cache



[After Andrei Pavlov 2018 & Intel]

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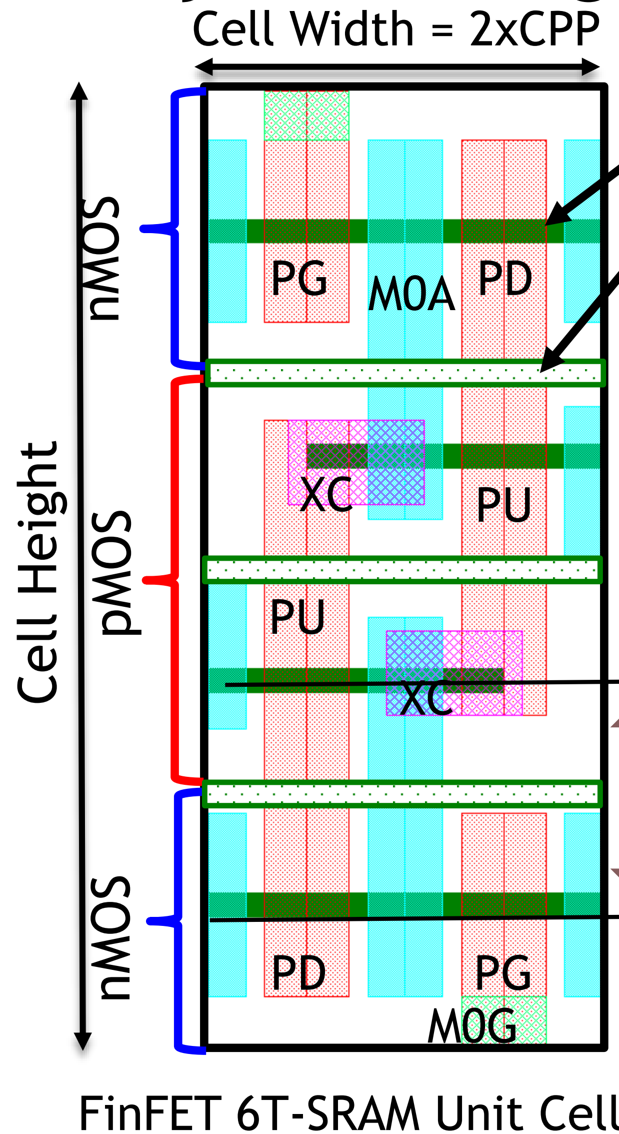
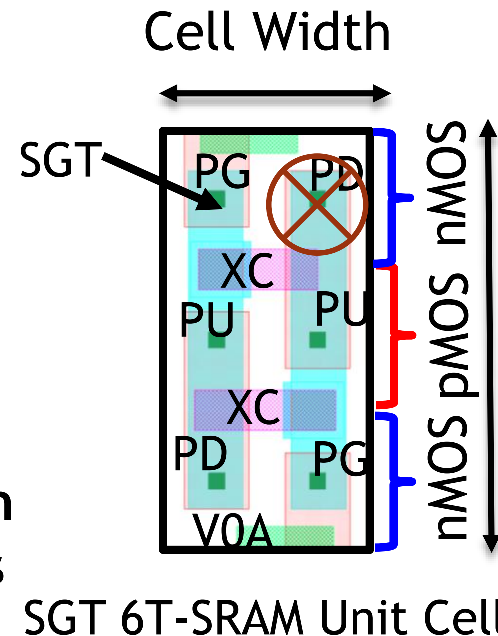
Key Advantage of SGT SRAM: Diffusion Break and Long L_G



FinFET 6T-SRAM Unit Cell

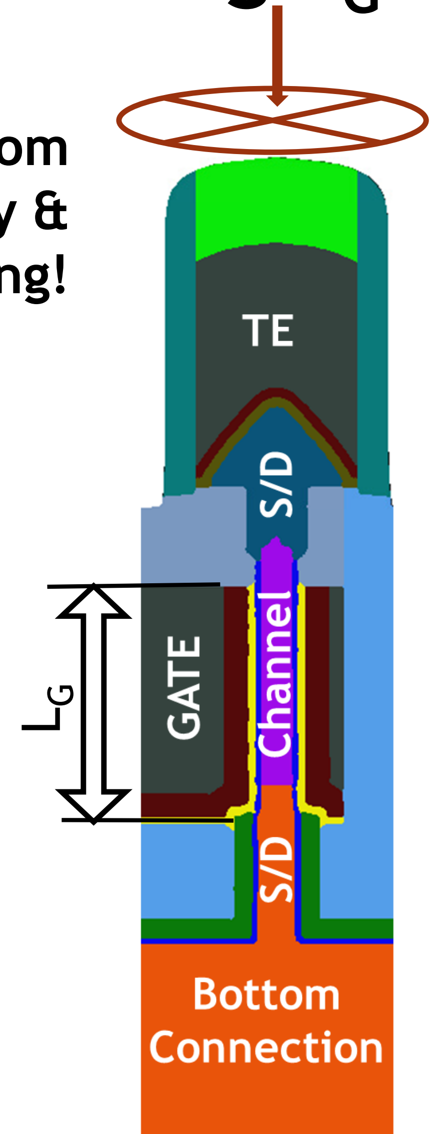
~3X area reduction thanks to no diffusion break in SGT cells (2FinPitch ~ double diffusion break between n/pMOS in *14nm* FinFET SRAM cell)

Further optimization can reduce area of SGT cells



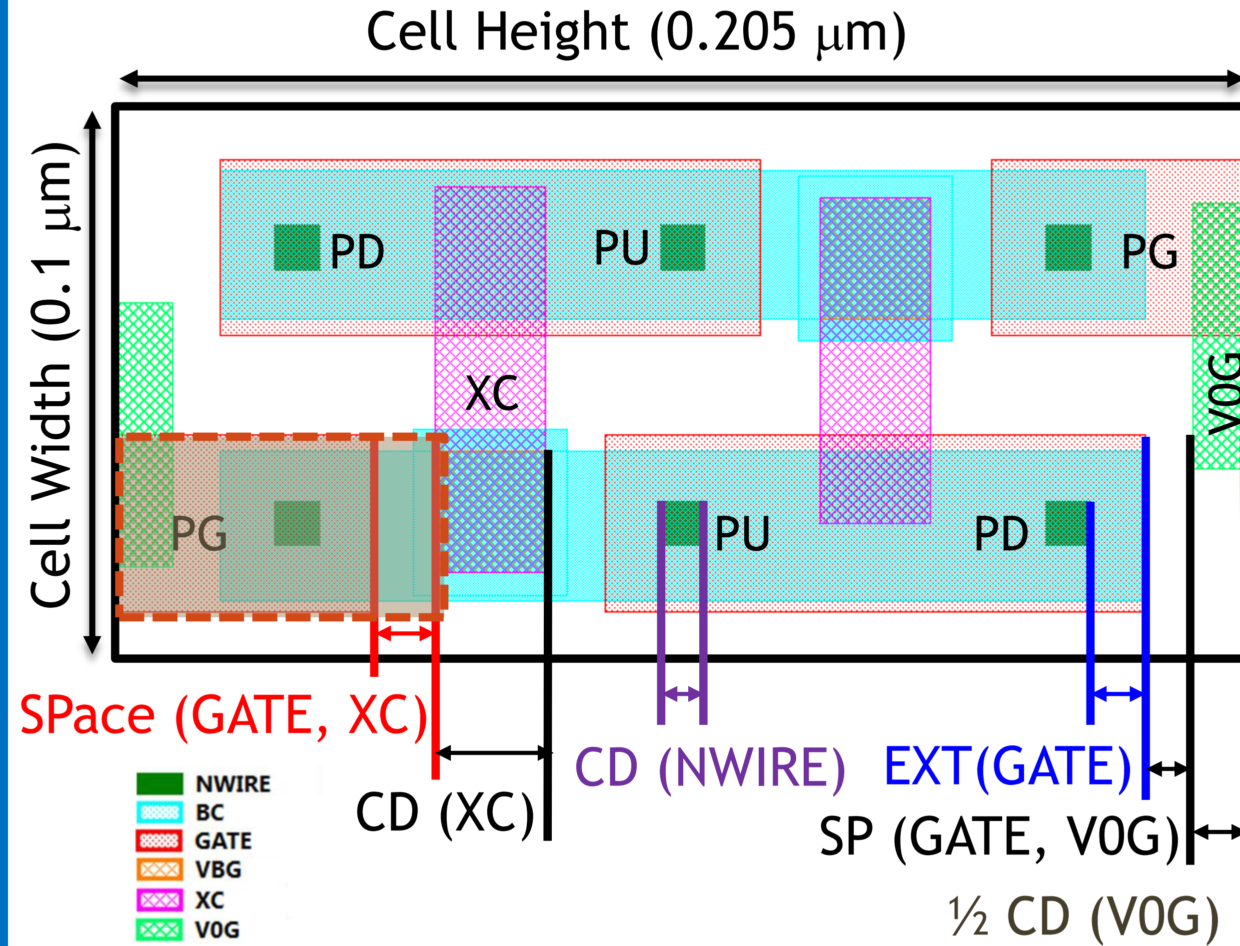
SGT 6T-SRAM Unit Cell

L_G decoupled from lithography & conventional scaling!



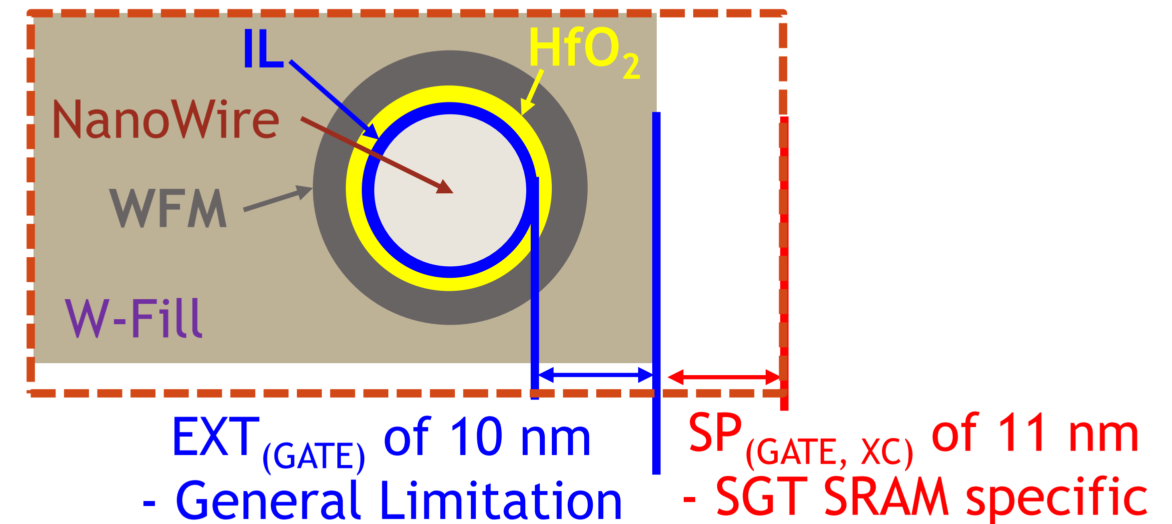
SGT SRAM Unit Cell Layout & Scaling Sensitive Parameters

SGT 6T-SRAM Unit Cell



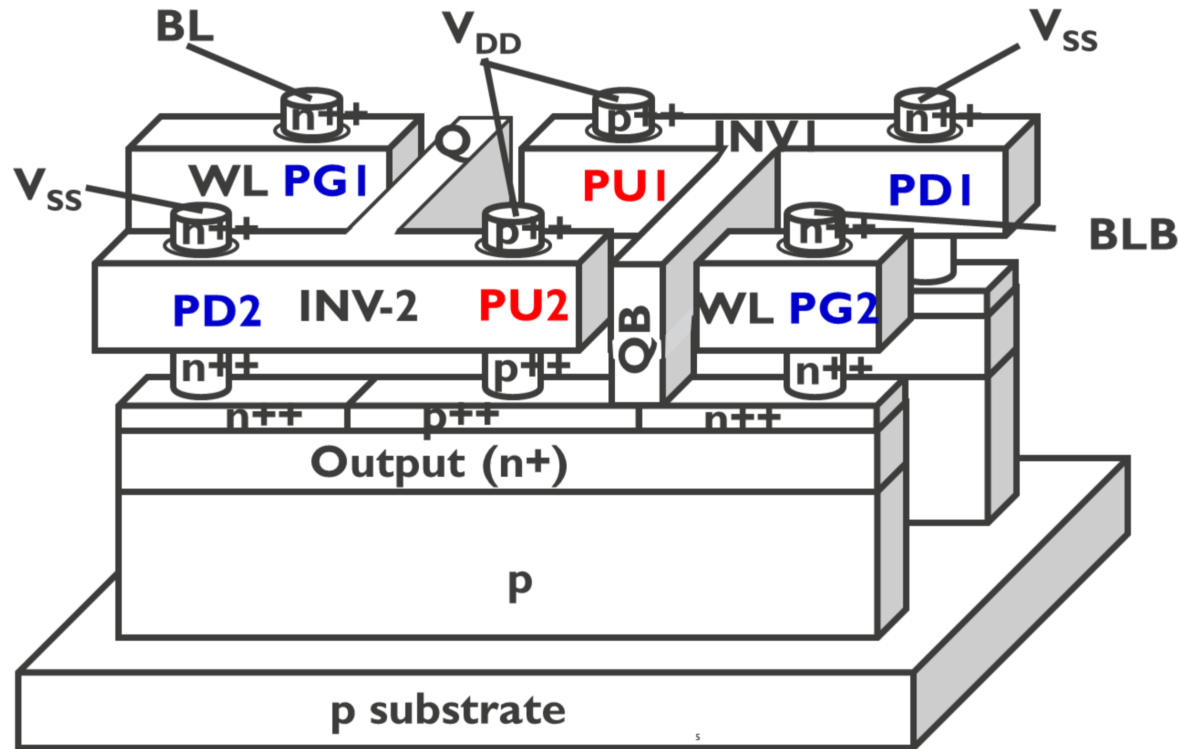
Scaling Sensitive Parameters

Cell Height	$3CD_{NW} + 6EXT_{GATE} + 2CD_{XC} + CD_{V0G} + 2SP_{(GATE,\ V0G)} + 4SP_{(GATE,\ XC)}$
Cell Width	$2CD_{NW} + 4EXT_{GATE} + 2SP_{(GATE,\ GATE)}$

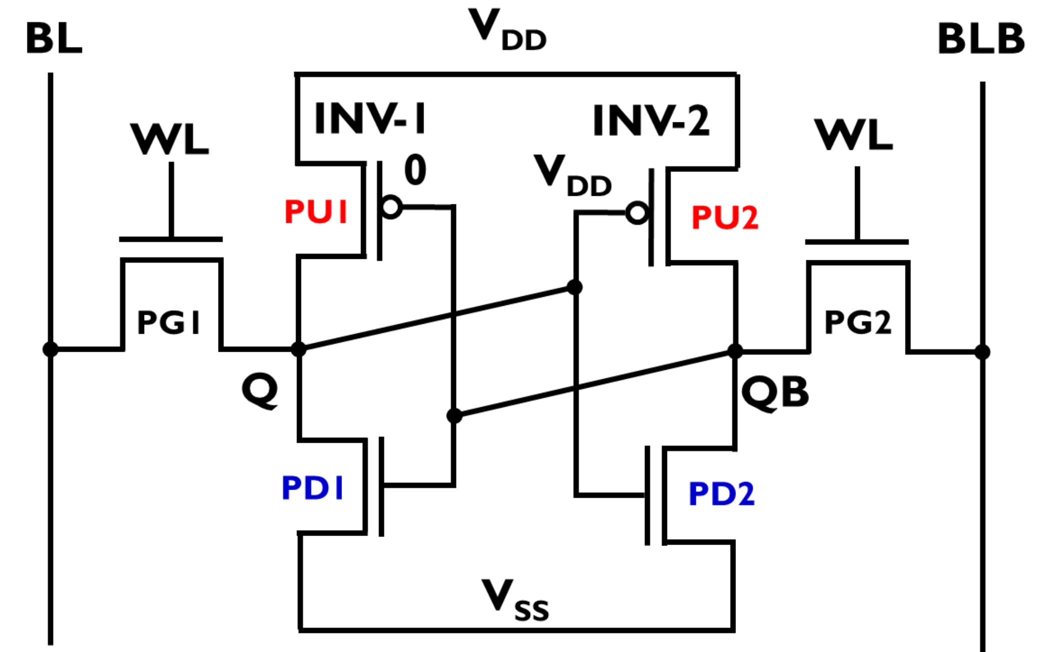


Bird's Eye View of 6T-SGT SRAM and its Equivalent Circuit

SGT SRAM unit cell with node 'Q' status is '1'



An equivalent SRAM circuit matching to 6-SGT SRAM



SGT SRAM DTCO and TCAD Simulation
[P. Matagne *et-al.*, SISPAD 2018]

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    - 5 EUV layers, 3 193i ArF layers
  - MOL / BEOL
    - 7 EUV layers, 1 193i ArF layer
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SGT SRAM Fabrication Process Steps: FEOL

- N-type Epi
- Bottom Junction [BPLUS]
- P-type channel Epi
- Nanowire pillars [NWIRE]
- Bottom Connection [BC]
- Bottom S/D (oxide recess)
- HK/MG-*first*
- Fill Metal Deposition & CMP
- Top S/D onset (W Recess)
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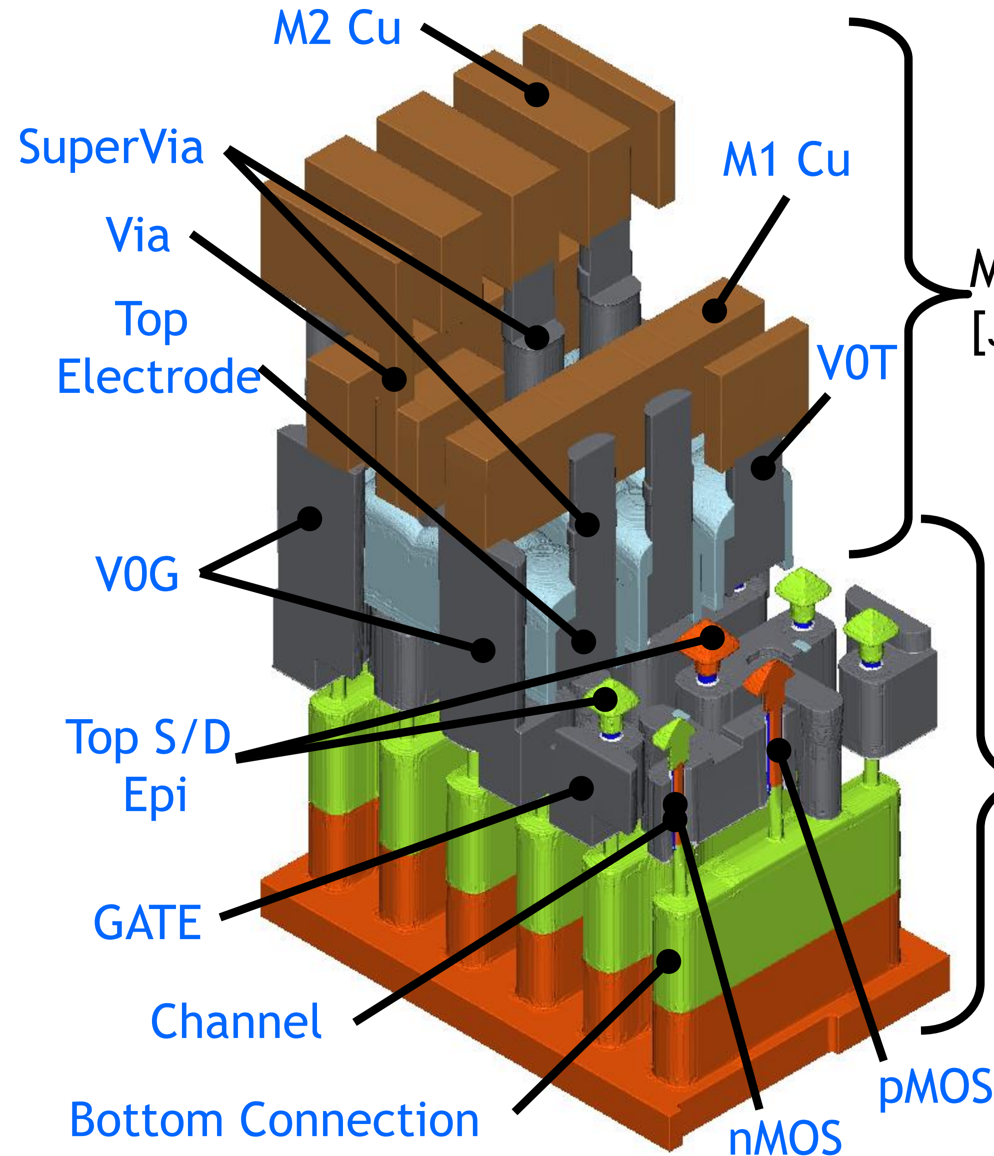

MOL / BEOL
[J. Bömmels *et-al.*, IITC 2019]

FEOL – the most disruptive building block for SGT

SGT SRAM Fabrication Process Steps: FEOL

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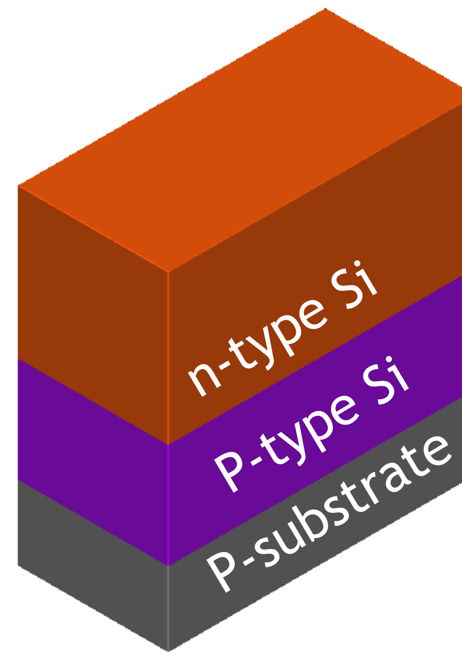

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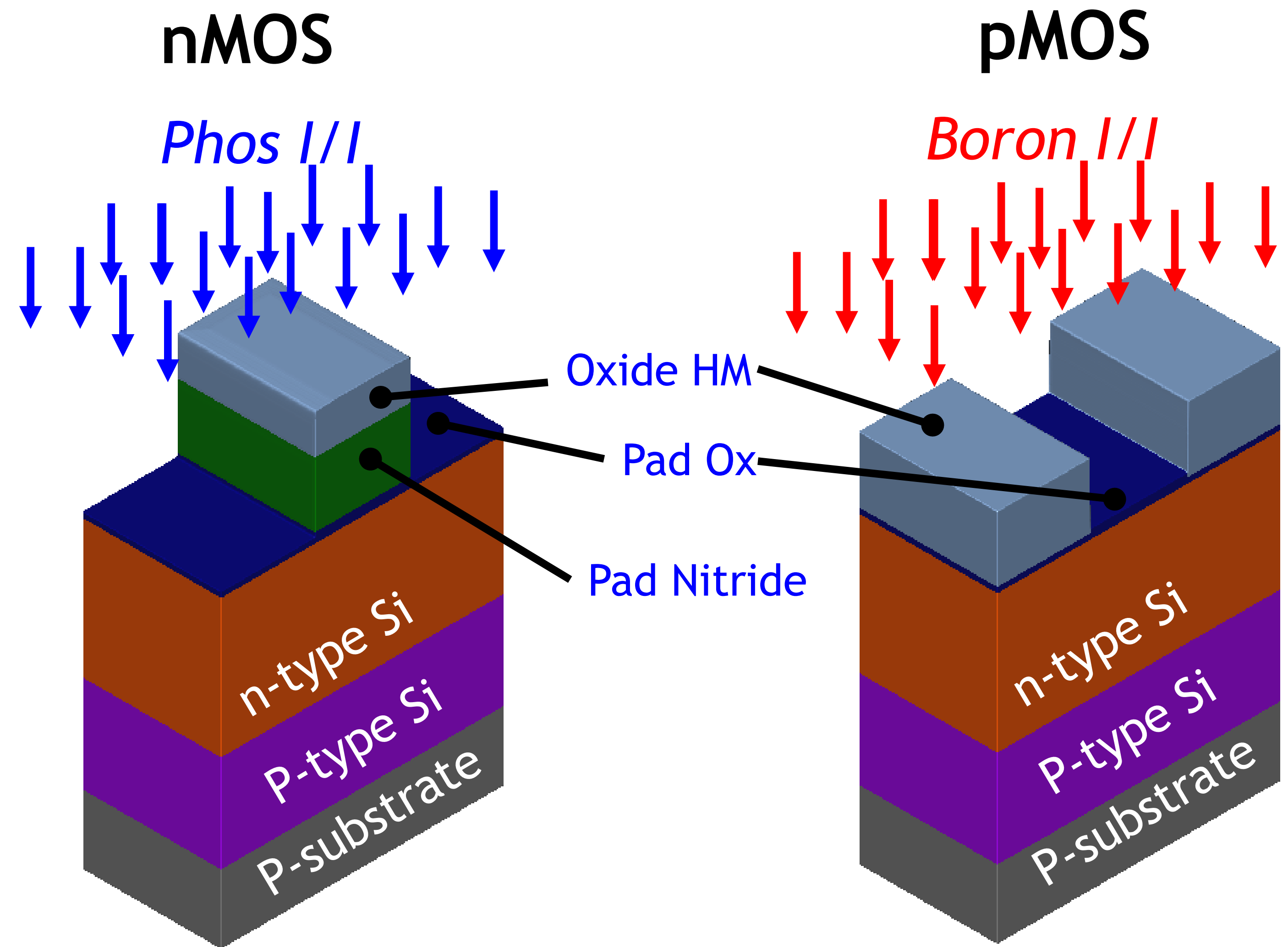

Hard-Mask based Self-Aligned Junction Formation

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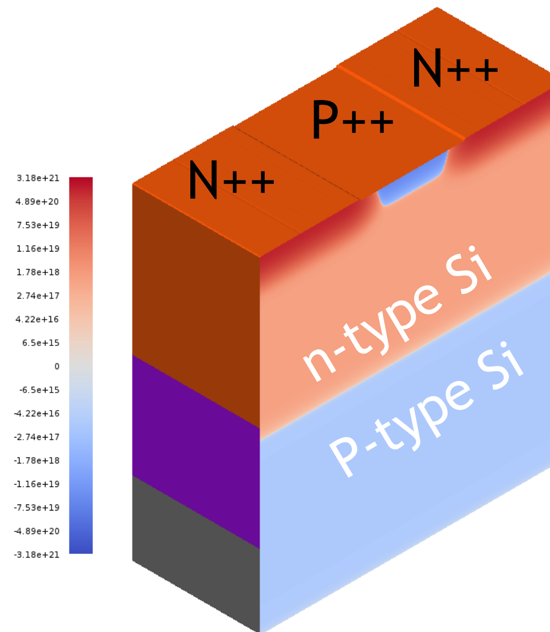

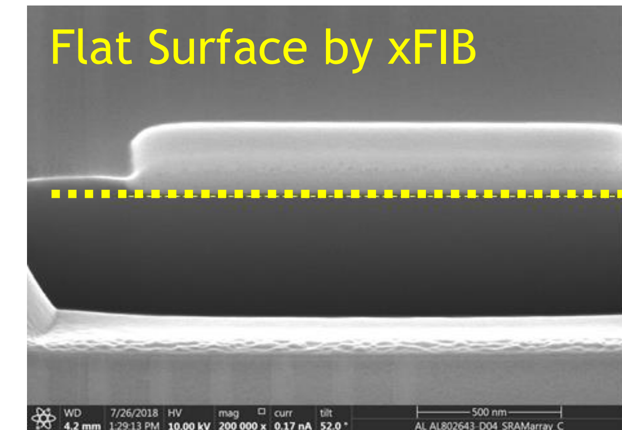

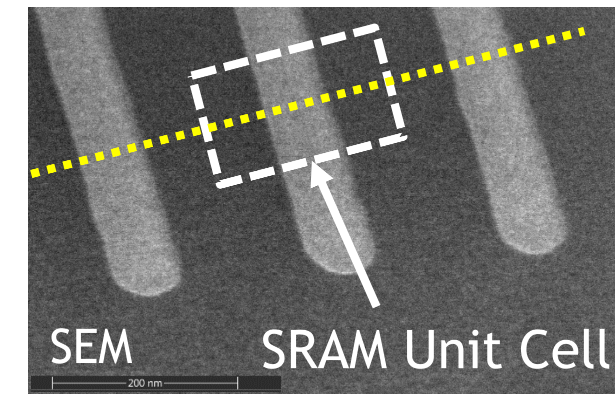

- Maintaining flat surface before channel Epi growth is important and is realized

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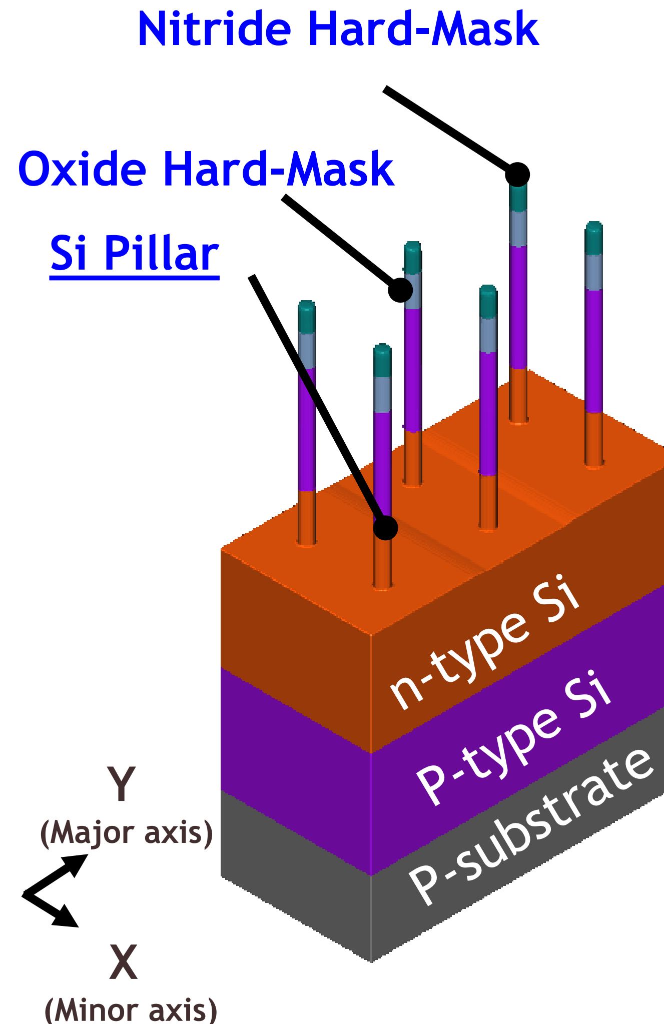
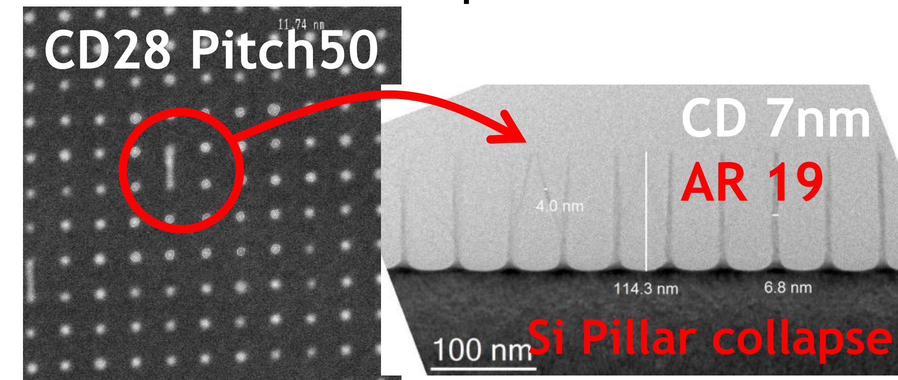
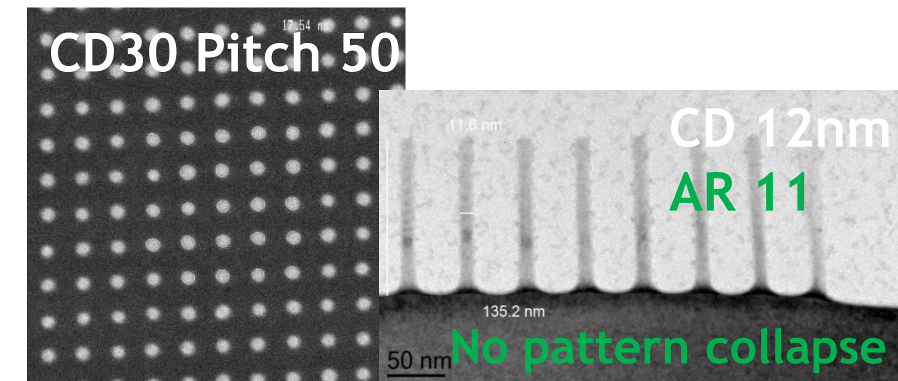


Si Pillar Pattern Collapse Test



When Aspect Ratio (AR) > AR_{crit}



When Aspect Ratio (AR) ≤ AR_{crit}

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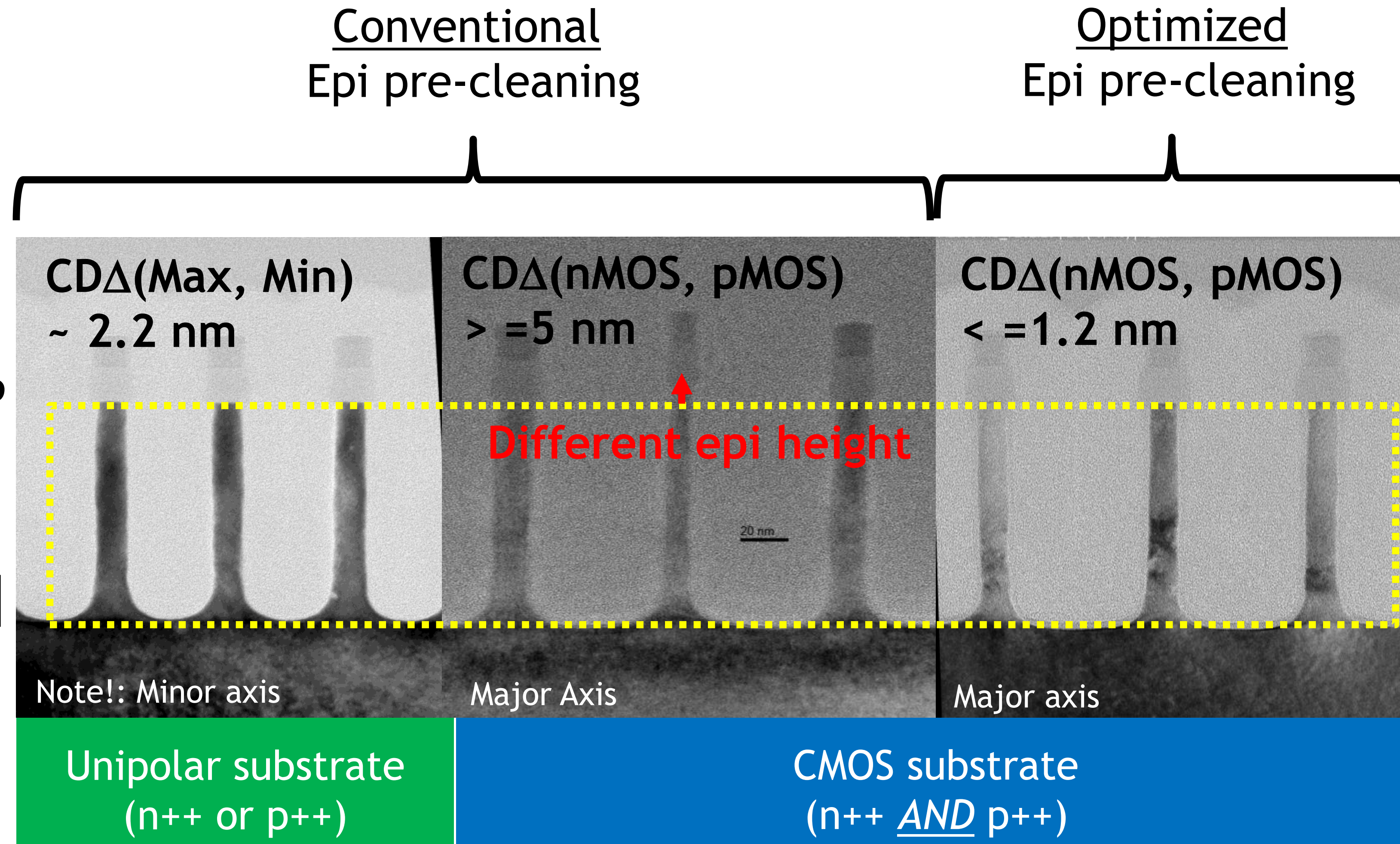

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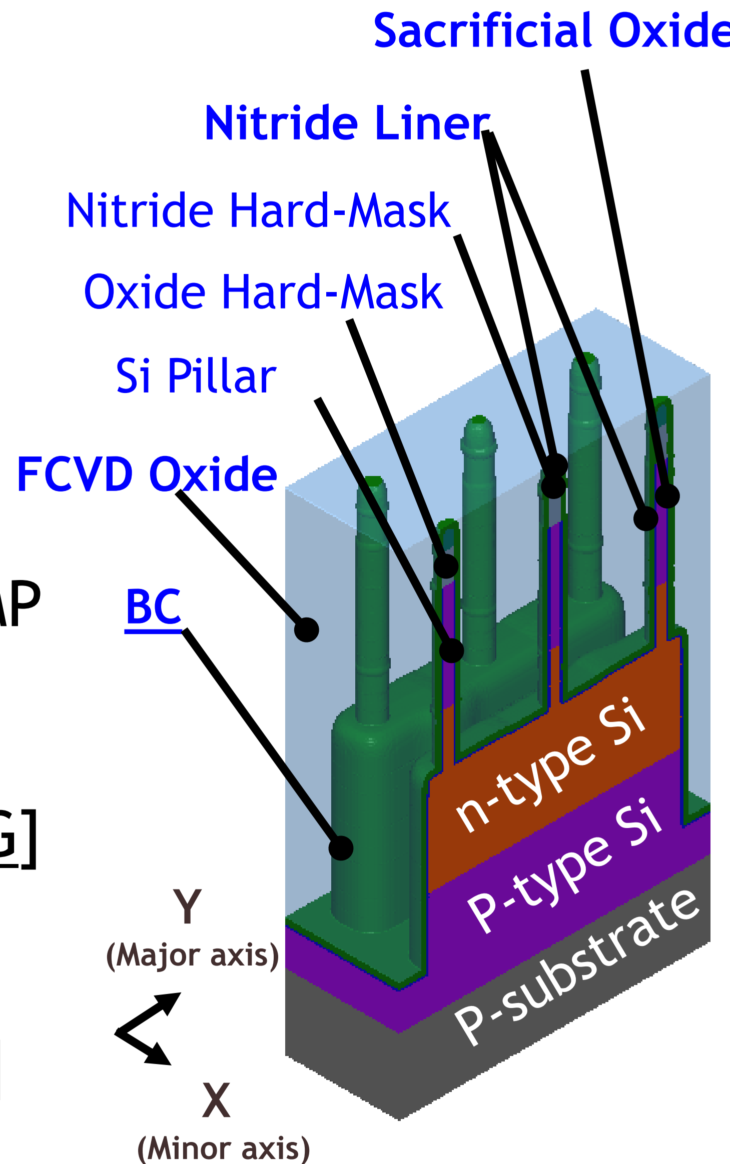
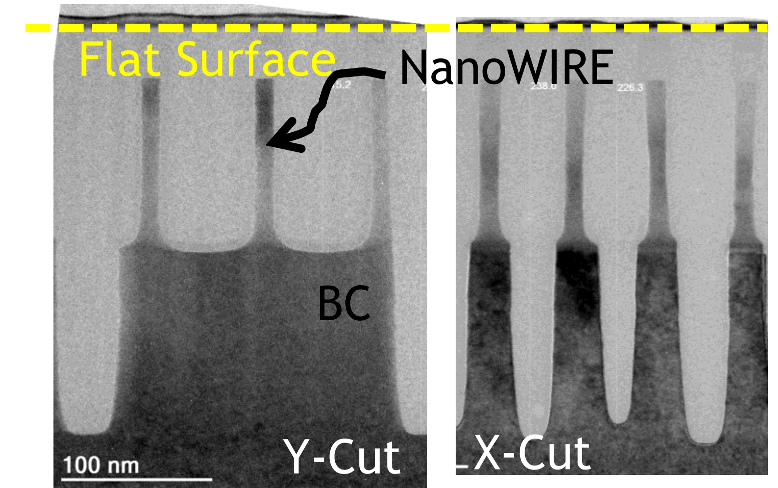
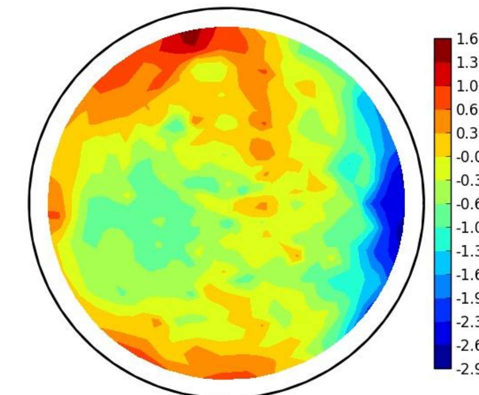


BC Oxide CMP stops @Nitride Liner



Typical OVL performance



|mean|+3σ ≤ 3 nm

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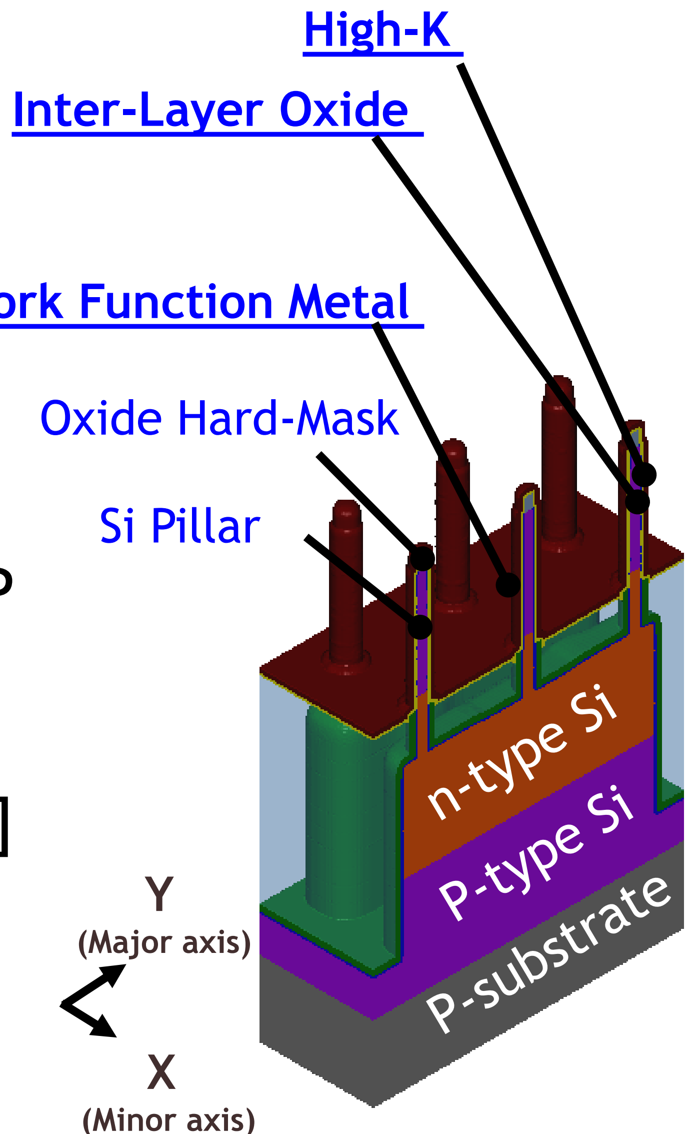
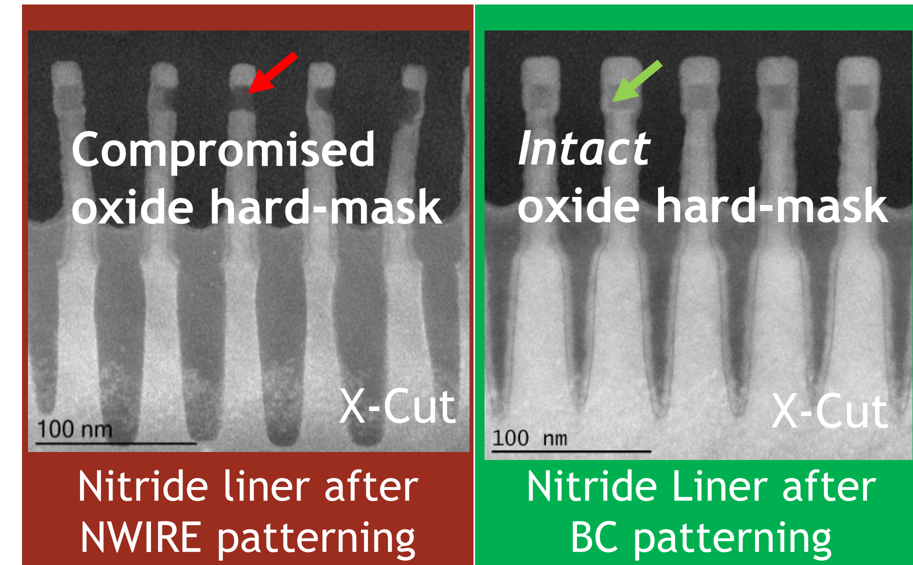
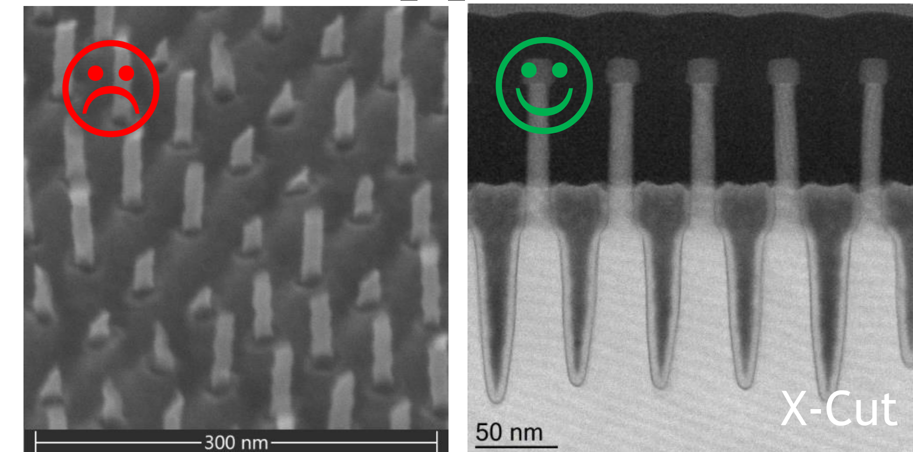


BHF *selective SiO_2 recess* against Si_3N_4



H_3PO_4 *selective Si_3N_4 removal* against SiO_2



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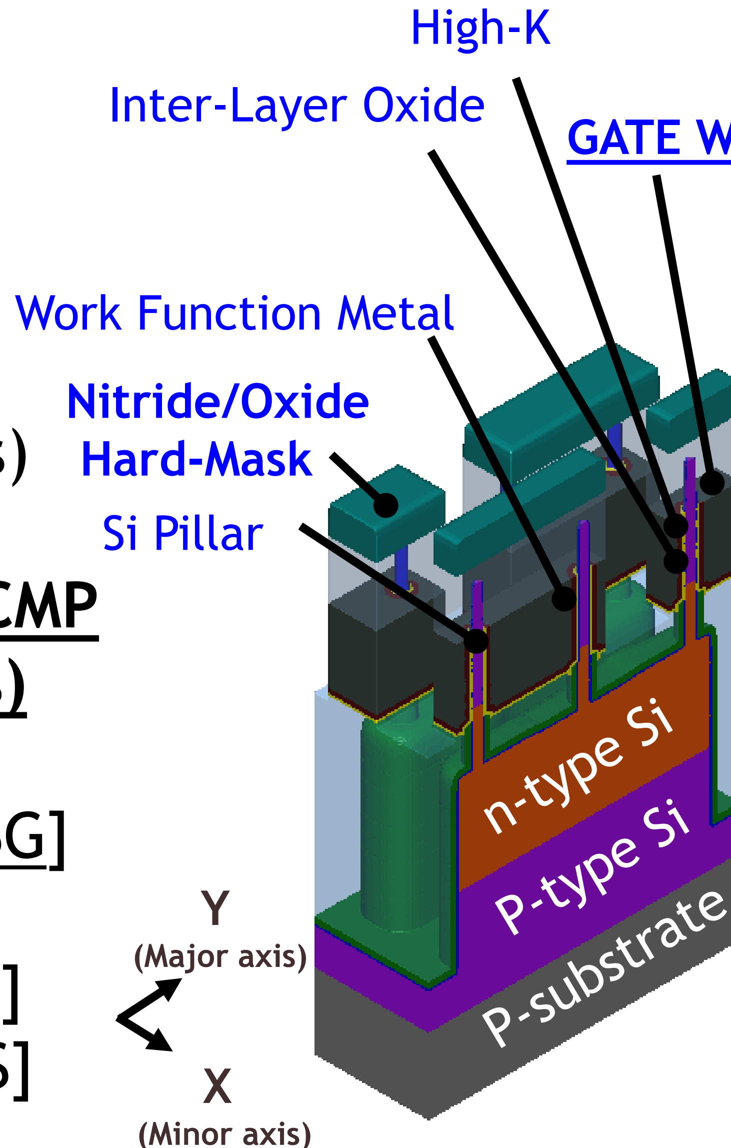
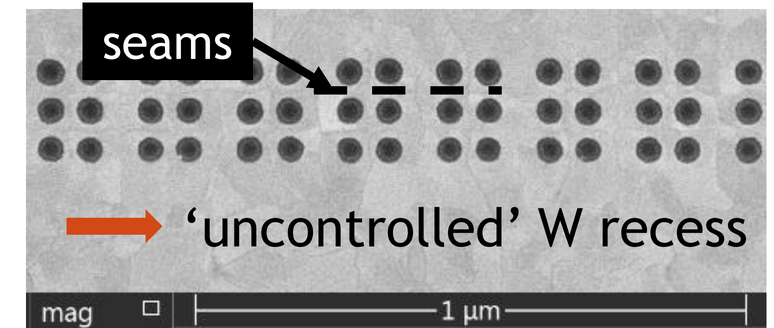
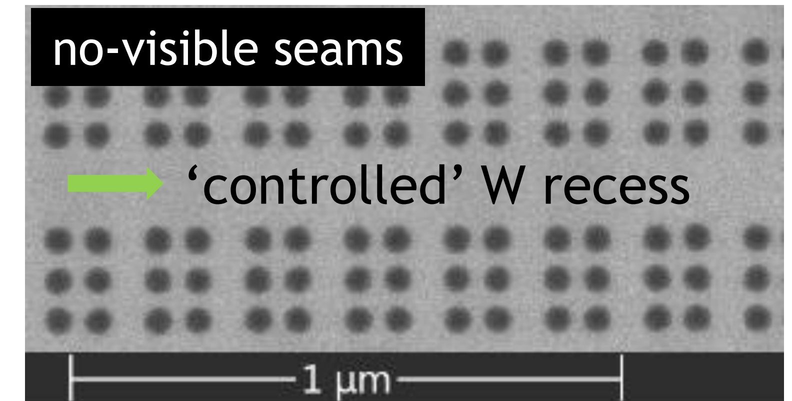


Post GATE W CMP with ***CVD W*** over fill



Post GATE W CMP with ***ALD W*** over fill



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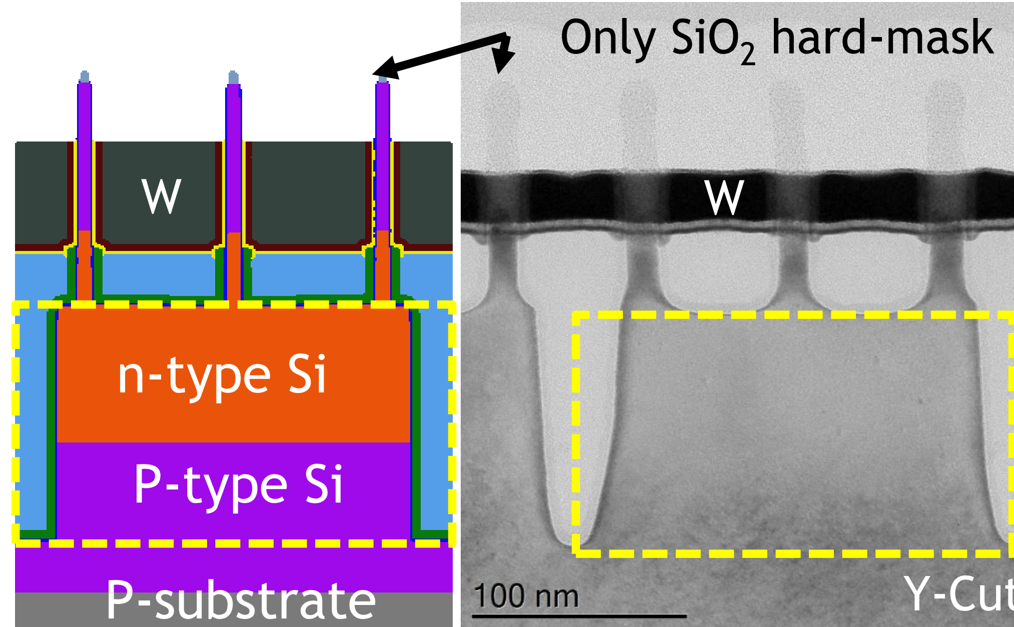
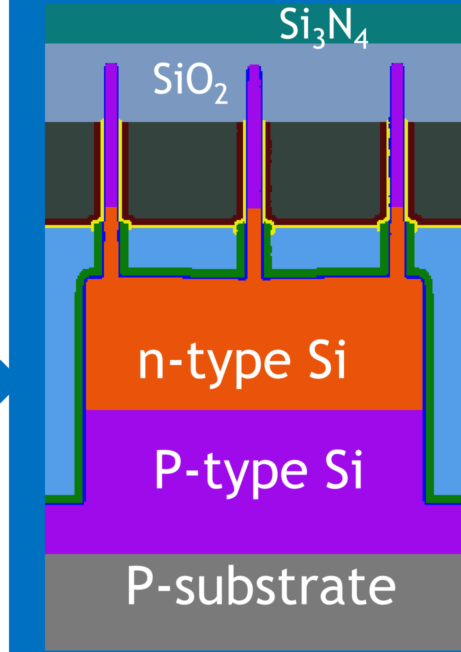
Post GATE W Recess Virtual vs. Real



Incoming to GATE module : No vertical self-alignment of top and bottom S/D to control under- / over-lap of gate



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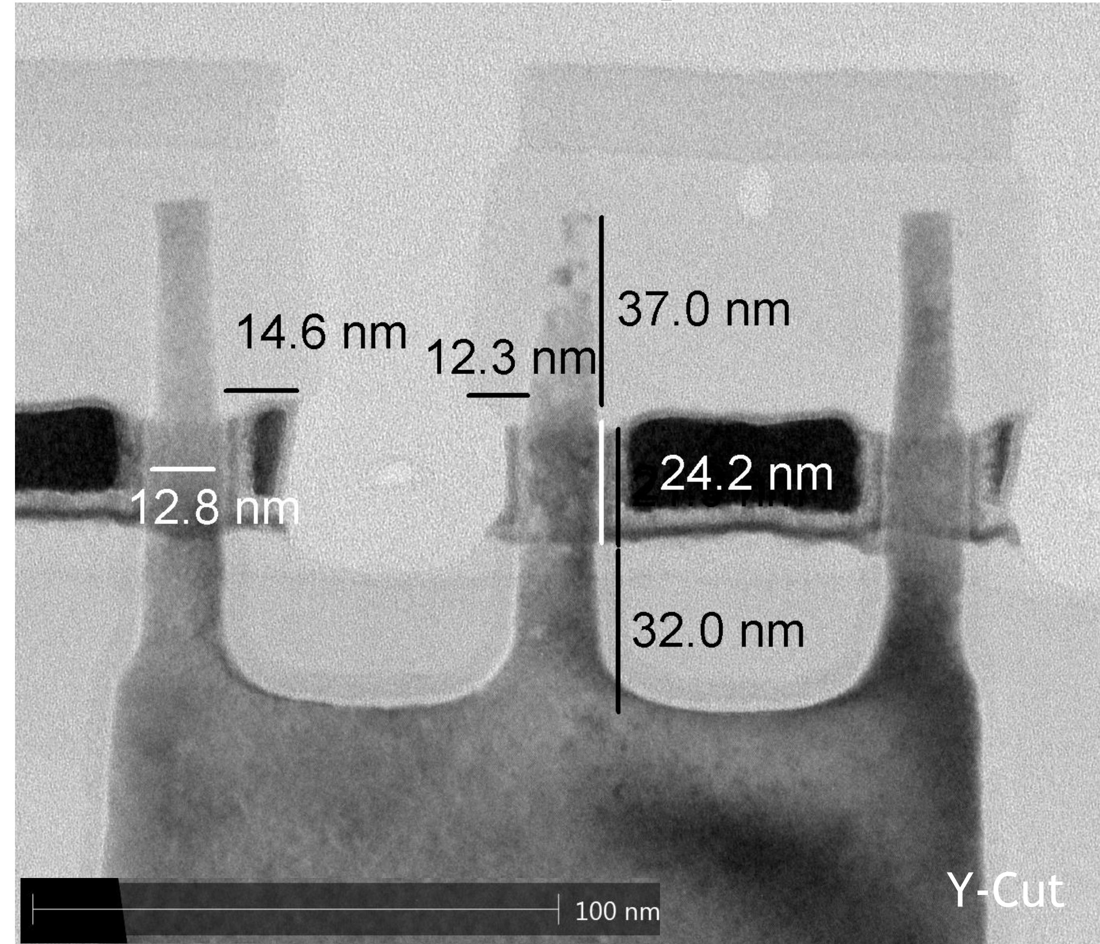

- GATE to NWIRE OVL is near perfect!
- GATE etch needs further improvement & is most challenging to cope with incoming variations not to compromise WFM TiN

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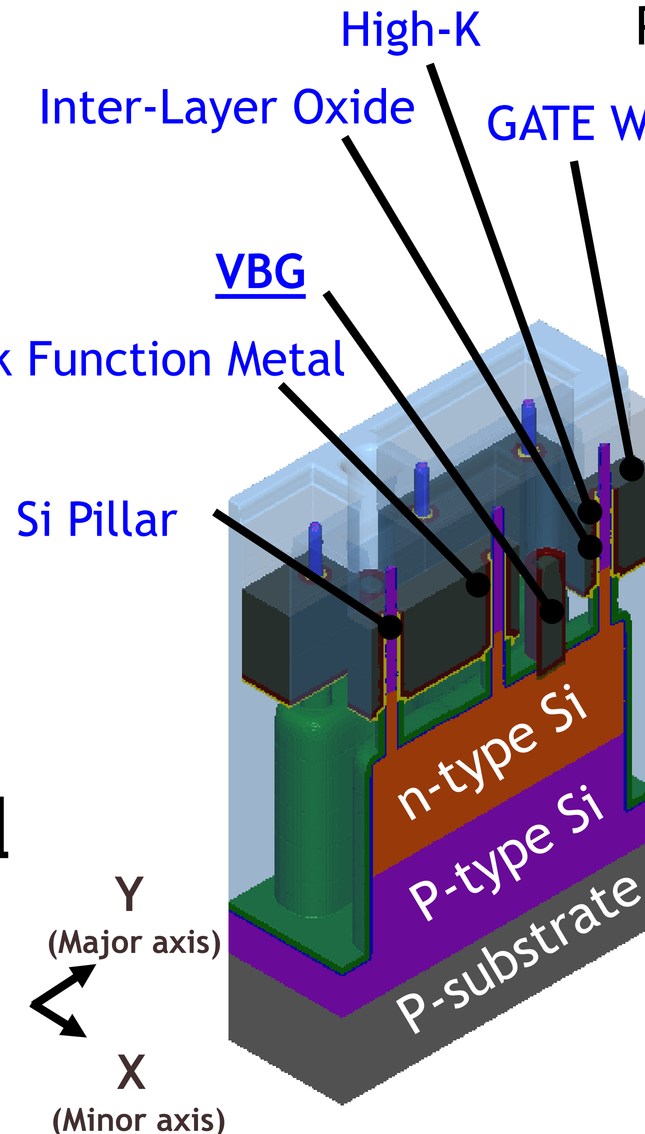
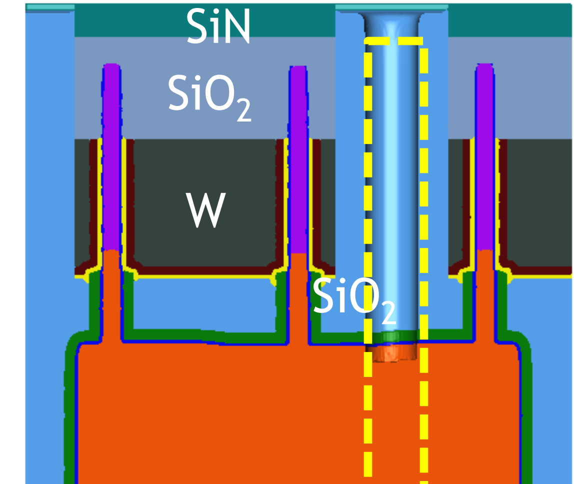
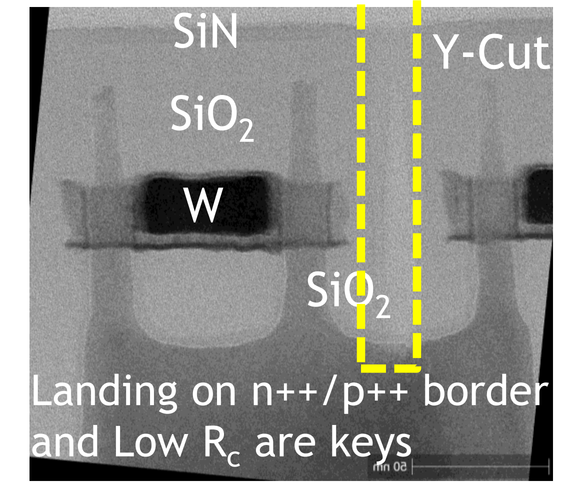


Post VBG Contact Etch Virtual vs. Real





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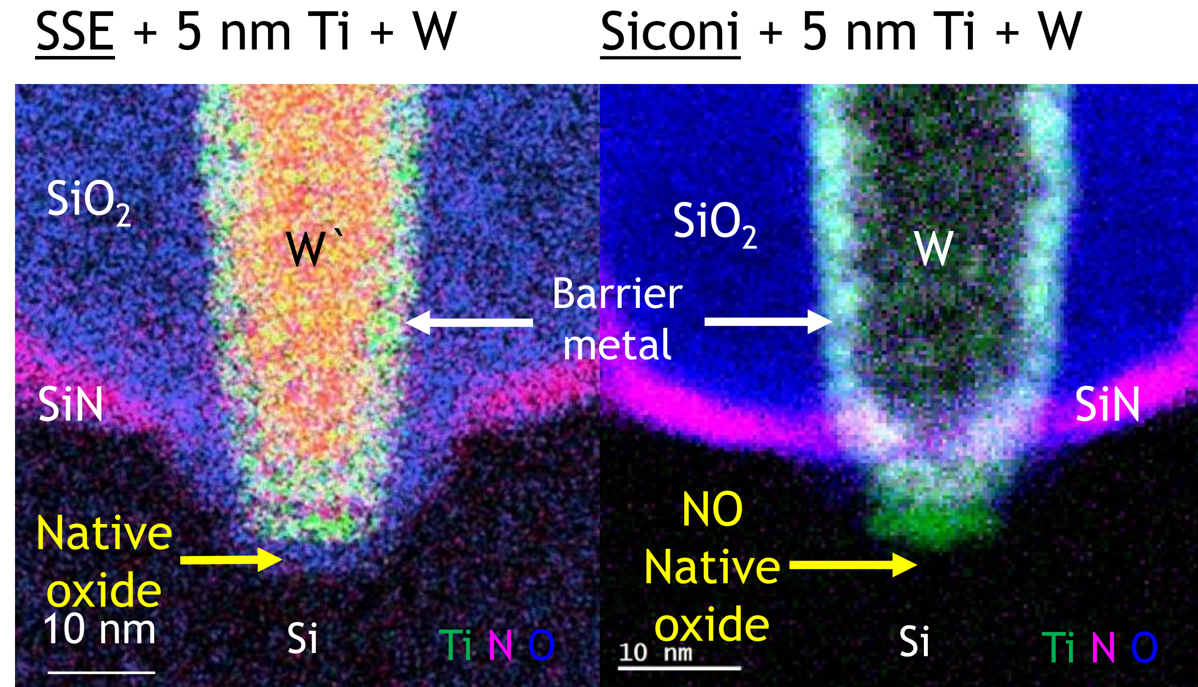
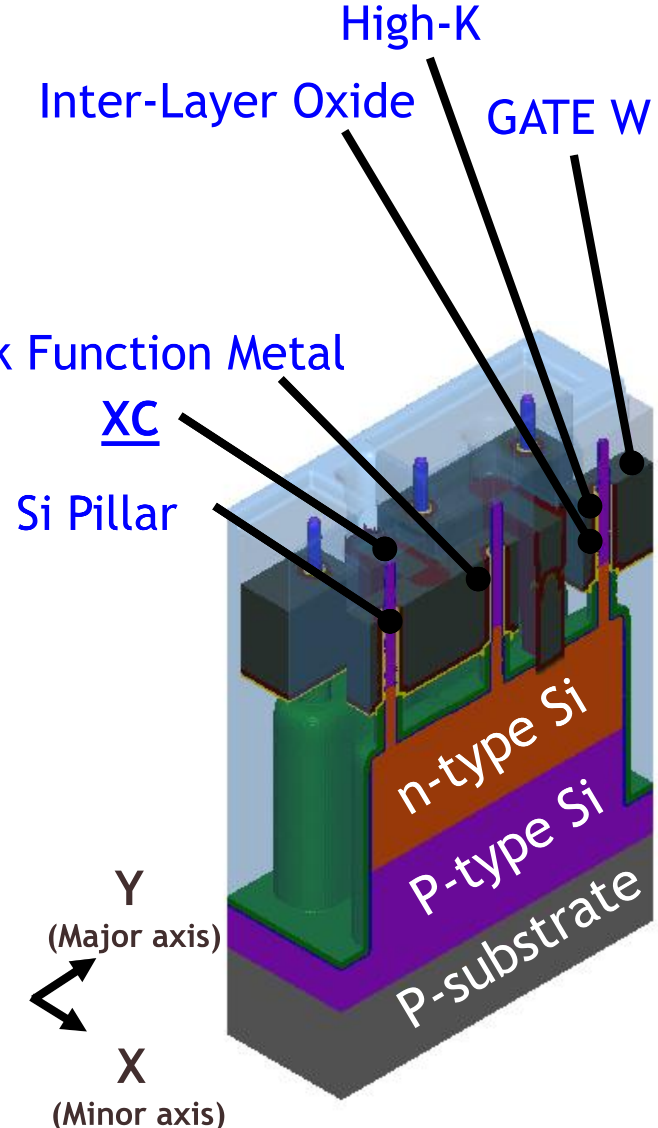
Optimization of imec *in-house* contact metallization scheme



- Native oxide removed by conventional Siconi pre-cleaning
- Lacking of exposed Si-sidewall coverage of PVD Ti can be further improved by ALD/CVD Ti (aligns to advanced wrap-around-contact)

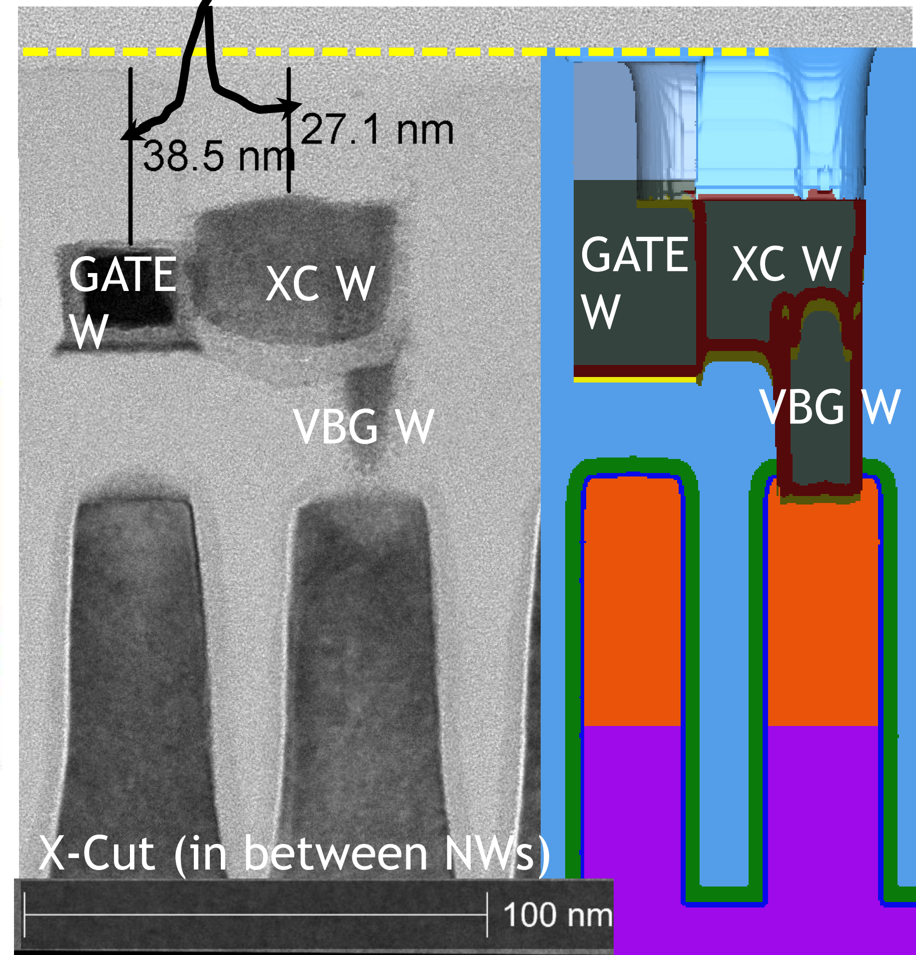
SGT SRAM Fabrication Process Steps: FEOL

- N-type Epi
- Bottom Junction [BPLUS]
- P-type channel Epi
- Nanowire pillars [NWIRE]
- Bottom Connection [BC]
- Bottom S/D (oxide recess)
- HK/MG-***first***
- Fill Metal Deposition & CMP
- Top S/D onset (W Recess)
- Gate [GATE]
- Bottom Gate Contact [VBG]
- **Cross Couple [XC]**
- PMOS Top S/D Epi [PPLUS]
- NMOS Top S/D Epi [NPLUS]



Real vs. Virtual

- SiO_2 budget here is *very* critical



SGT SRAM Fabrication Process Steps: FEOL

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- **PMOS Top S/D Epi [PPLUS]**
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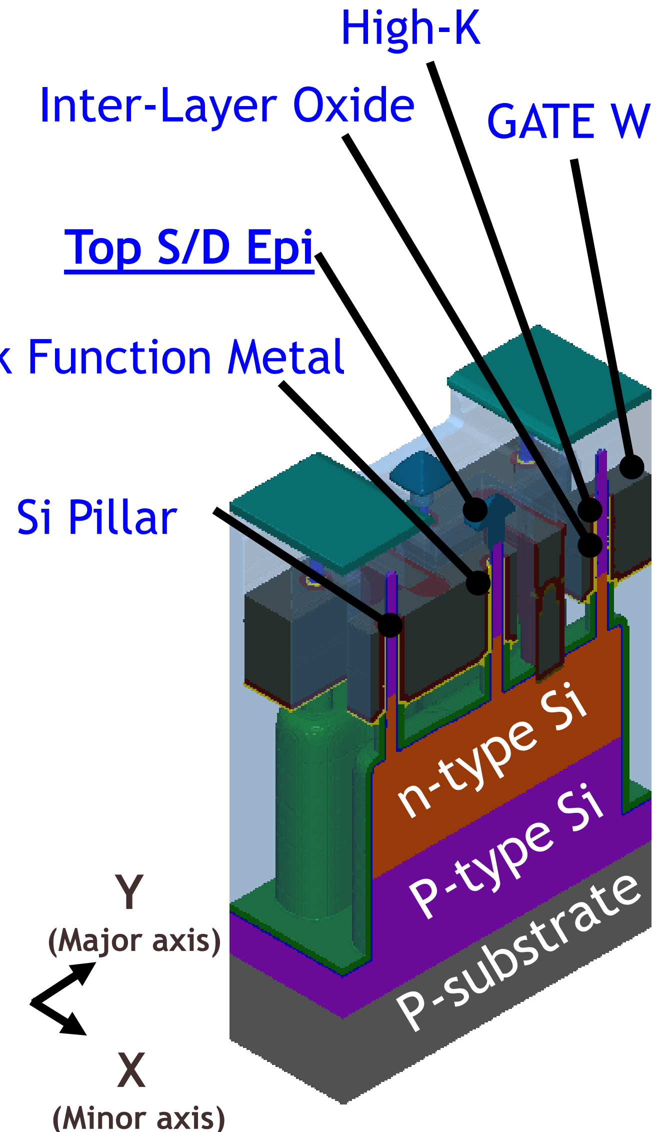
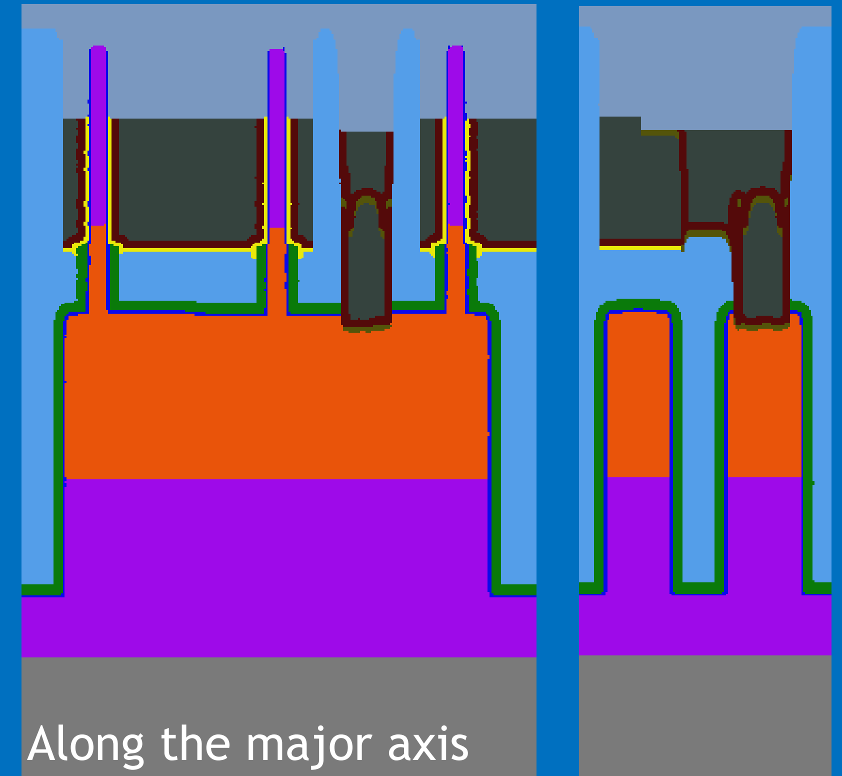


Incoming to Top S/D Epi module : No vertical self-alignment - we don't want metal in the Epi reactor.



SGT SRAM Fabrication Process Steps: FEOL

- N-type Epi
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- Nanowire pillars [NWIRE]
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- Bottom S/D (oxide recess)
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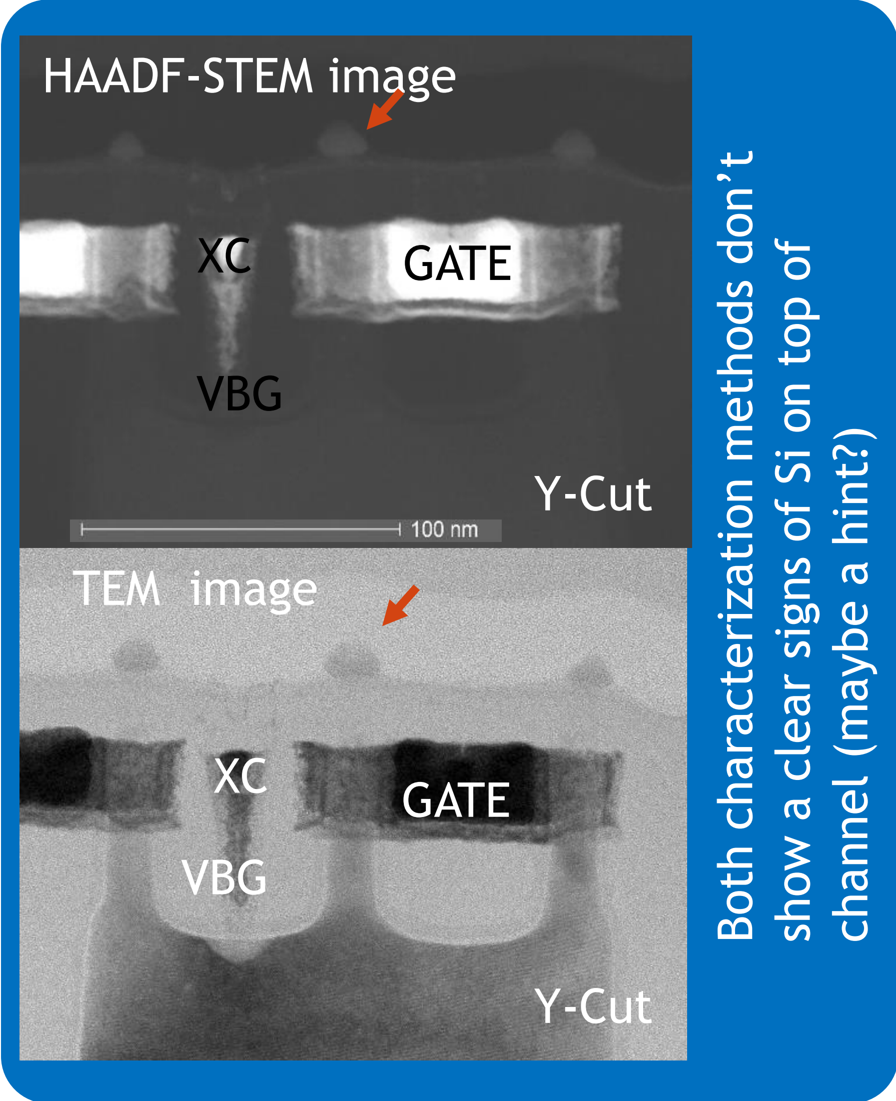
- Bottom Gate Contact [VBG]
- Cross Couple [XC]
- **PMOS Top S/D Epi [PPLUS]**
- **NMOS Top S/D Epi [NPLUS]**

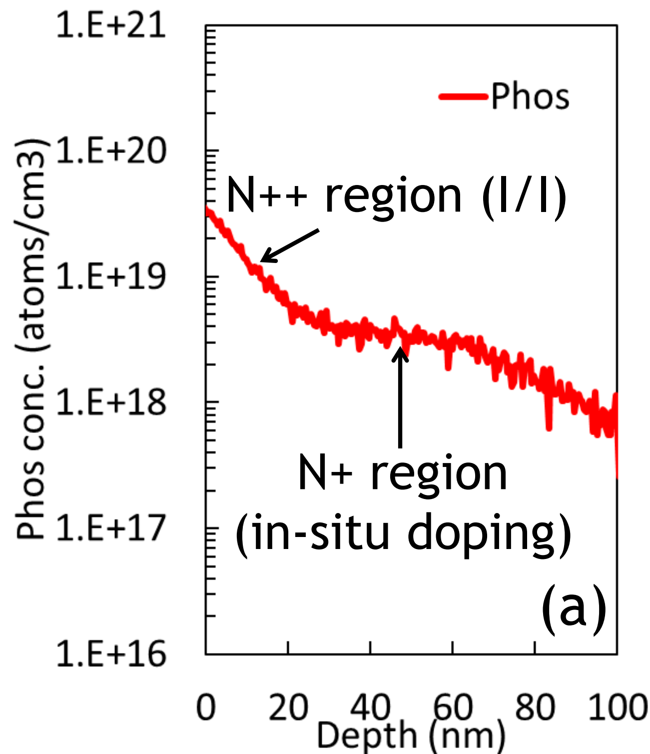
Top S/D Epi from uni-channel device lot

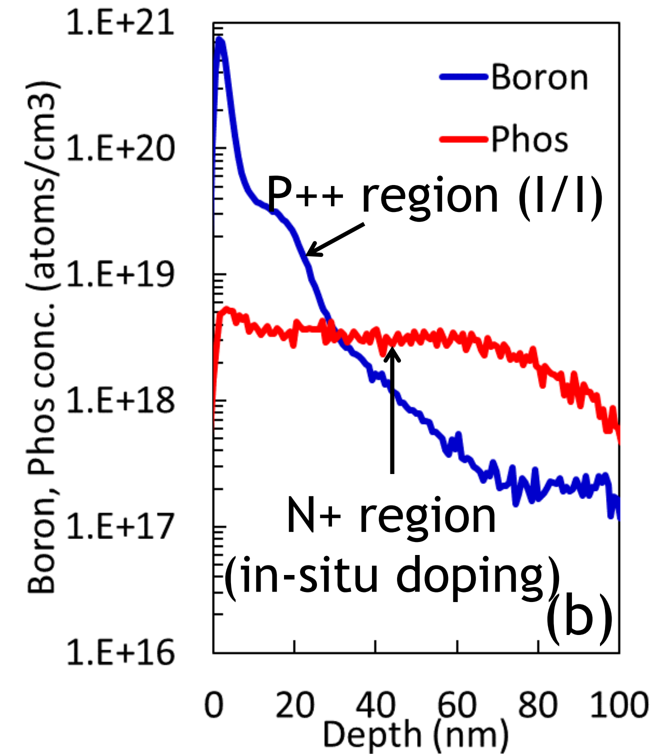


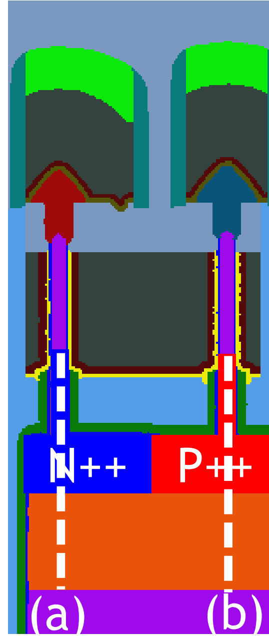
SGT SRAM Fabrication Process Steps: FEOL, Junctions

- N-type Epi
- Bottom Junction [BPLUS]
- P-type channel Epi
- Nanowire pillars [NWIRE]
- Bottom Connection [BC]
- Bottom S/D (oxide recess)
- HK/MG-*first*
- Fill Metal Deposition & CMP
- Top S/D onset (W Recess)
- Gate [GATE]
- Bottom Gate Contact [VBG]
- Cross Couple [XC]
- PMOS Top S/D Epi [PPLUS]
- **NMOS Top S/D Epi [NPLUS]**

SIMS depth profile of N++ region and P++ region







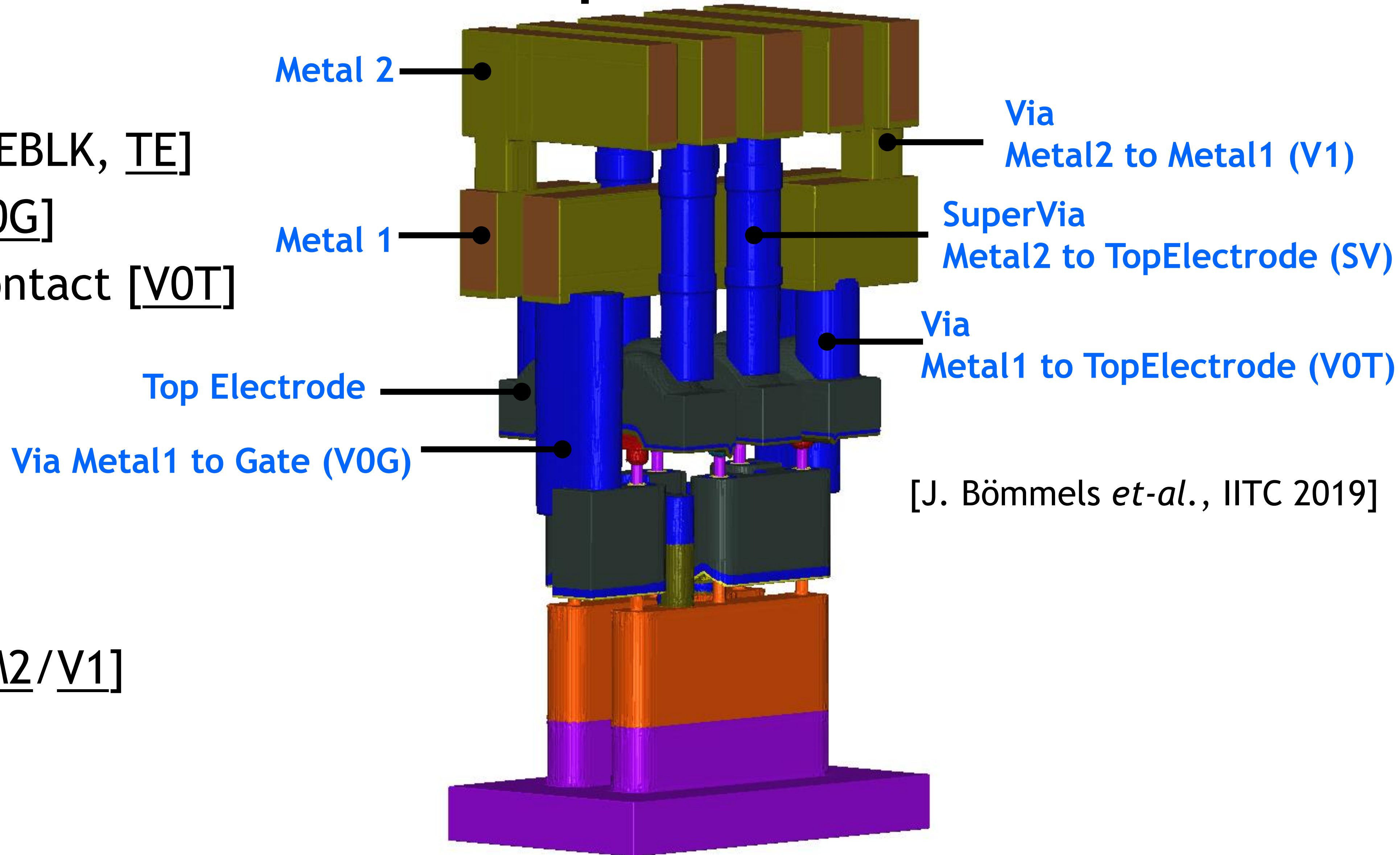
SGT SRAM Process Steps: MOL / BEOL

MOL

- Top Electrode [TEBLK, TE]
- Gate Contact [V0G]
- Top Electrode Contact [V0T]

BEOL

- Metal 1 [M1]
- Super Via [SV1]
- Metal 2 / Via1 [M2/V1]



[J. Bömmels *et-al.*, IITC 2019]

SGT SRAM Process Steps: MOL / BEOL

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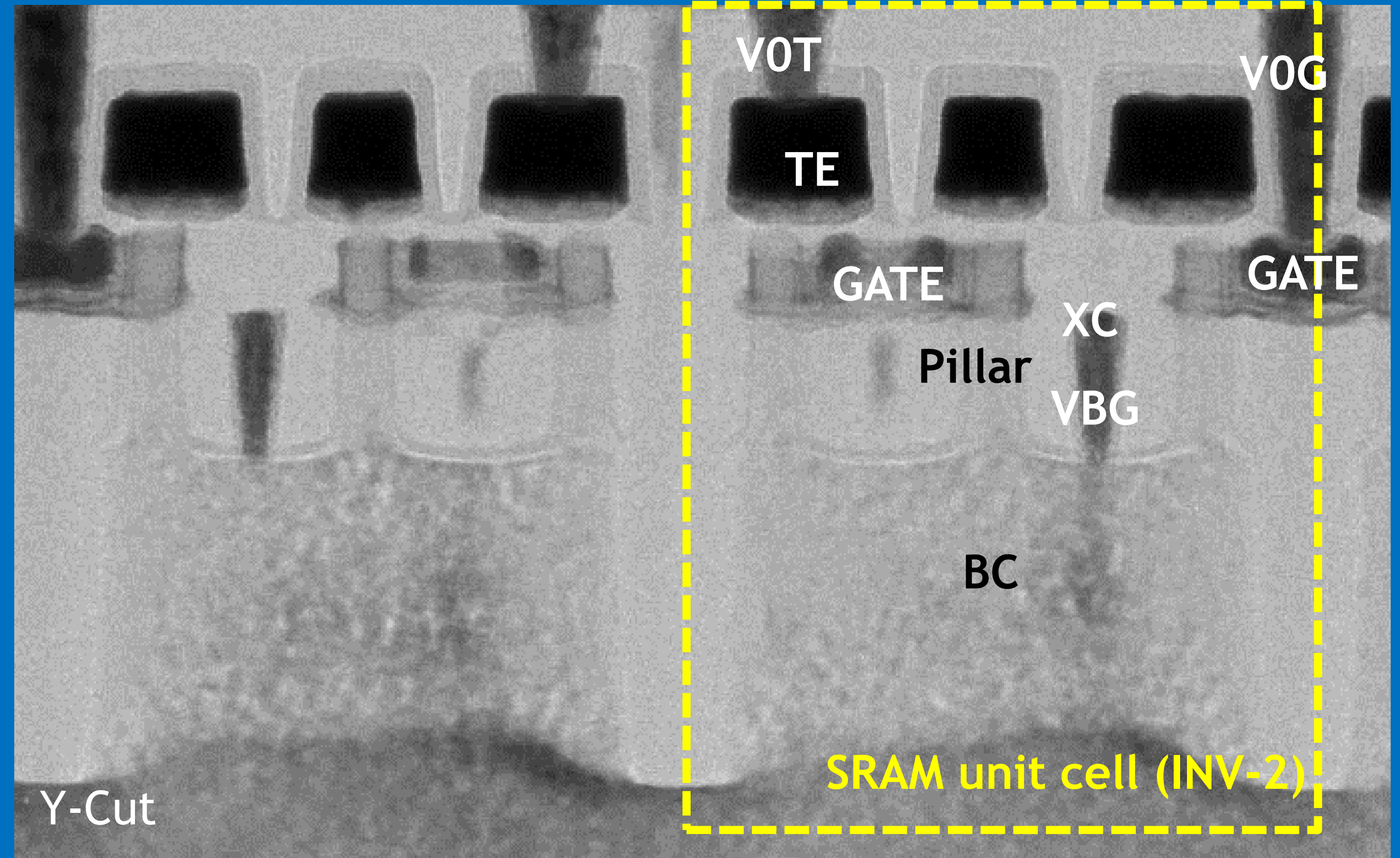
BEOL

- Metal 1 [M1]
- Super Via [SV1]
- Metal 2 / Via1 [M2/V1]

XTEM from 1st Device Wafer @M1



SGT SRAM Process Steps: MOL / BEOL

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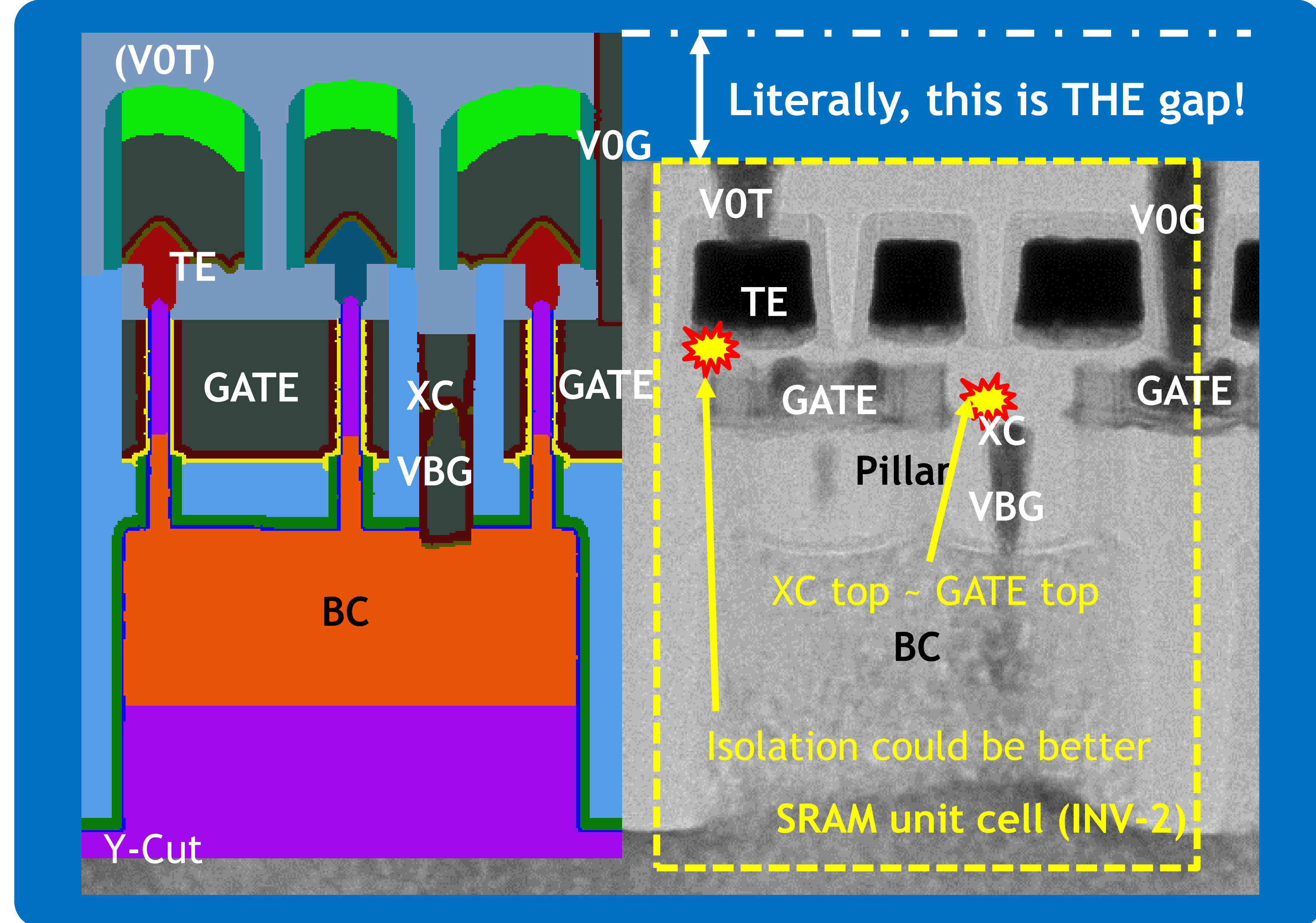
Gap Analysis

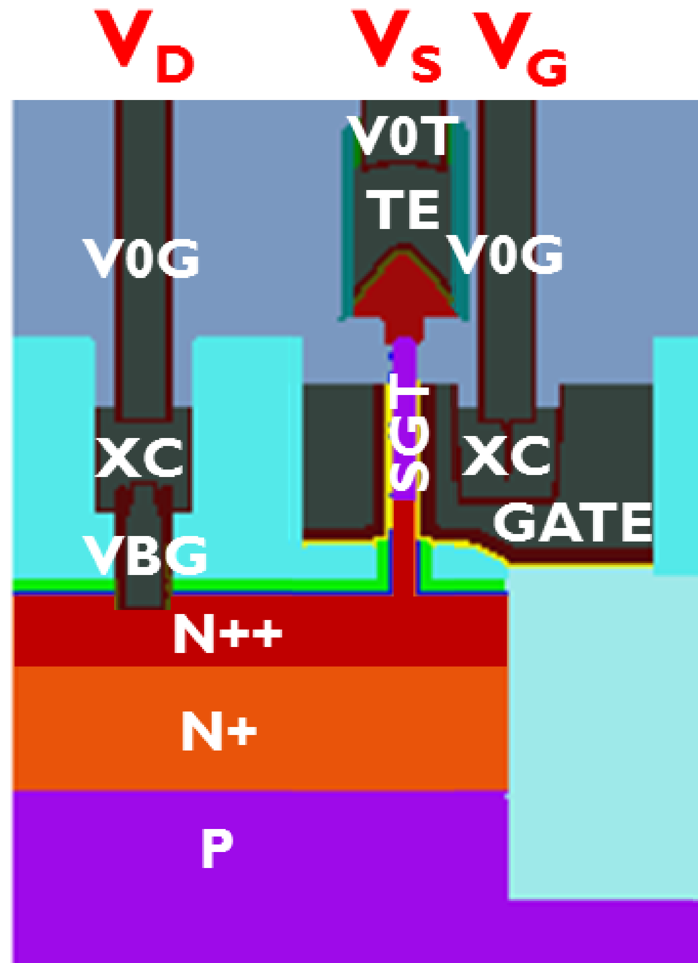


Outline

- Motivation
- SGT 6-T SRAM Key Design & SRAM Equivalent Circuit
- SGT SRAM Process Steps & Process Optimization
  - FEOL
  - MOL / BEOL
- Device Characterization
- Summary & Outlook

nMOS functioning I_D-V_G curves from the 1st SGT device wafer

Stand-Alone Device configuration



I_D-V_G characteristics

NW diameter: 8 nm
Physical L_G: 21 nm

V_D = 0.8 V
V_D = 0.05 V

I_D [a.u.]

V_G [V]

0.0 0.2 0.4 0.6 0.8 1.0 1.2

V_{th} = 0.61 V
S.S._sat: 125 mV/dec
Ion / Ioff ~ 4 decades

Outline

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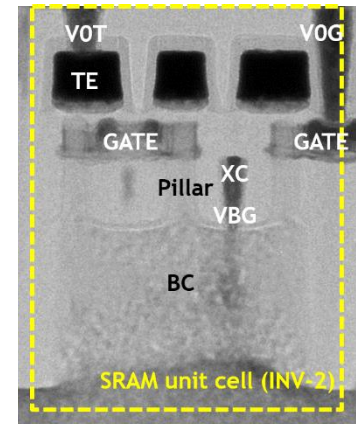
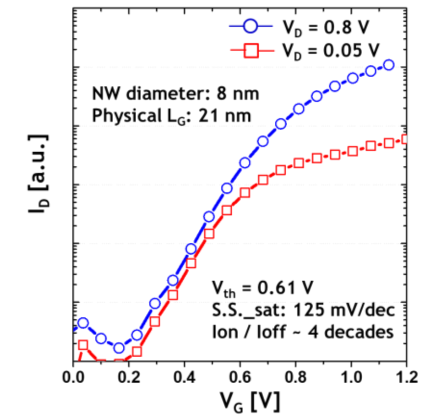
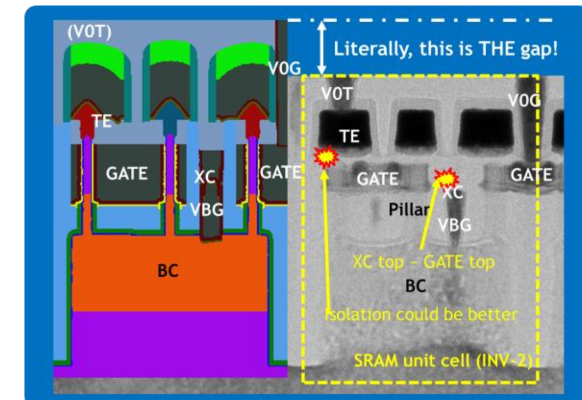
Summary & Outlook

- Summary
  - We established a fabrication process flow of a 5 nm-class, EUV-era ultra-density 6-SGT SRAM with 0.0205 μm^2 unit cell area by adapting DTCO, TCAD simulation, complimented by Coventor™ SEMulator®
  - Demonstrated nMOS SGT function from the very 1st device lot (unipolar)

- Outlook
  - Further optimize process integration flow and demonstrate *both* nMOS/pMOS SGT functional devices
  - Demonstrate full SRAM functionality & reliability test

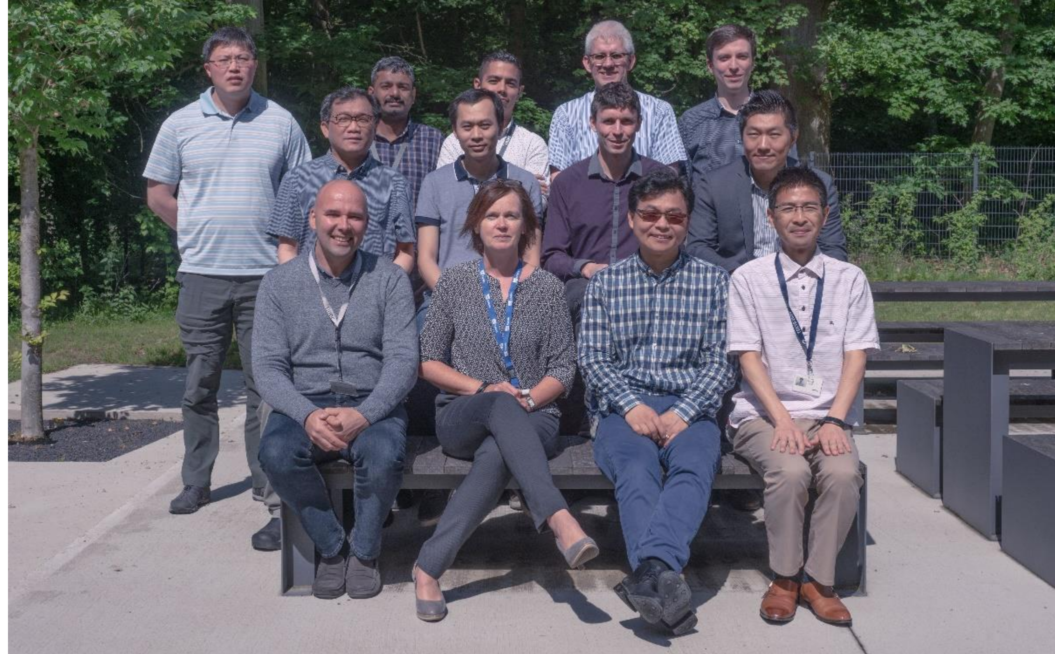






Acknowledgement

- The authors gratefully acknowledge imec DOT, MCA, SEMTEM, ILIME, Arenberg 300mm pilot line, and AMSIMEC for their support



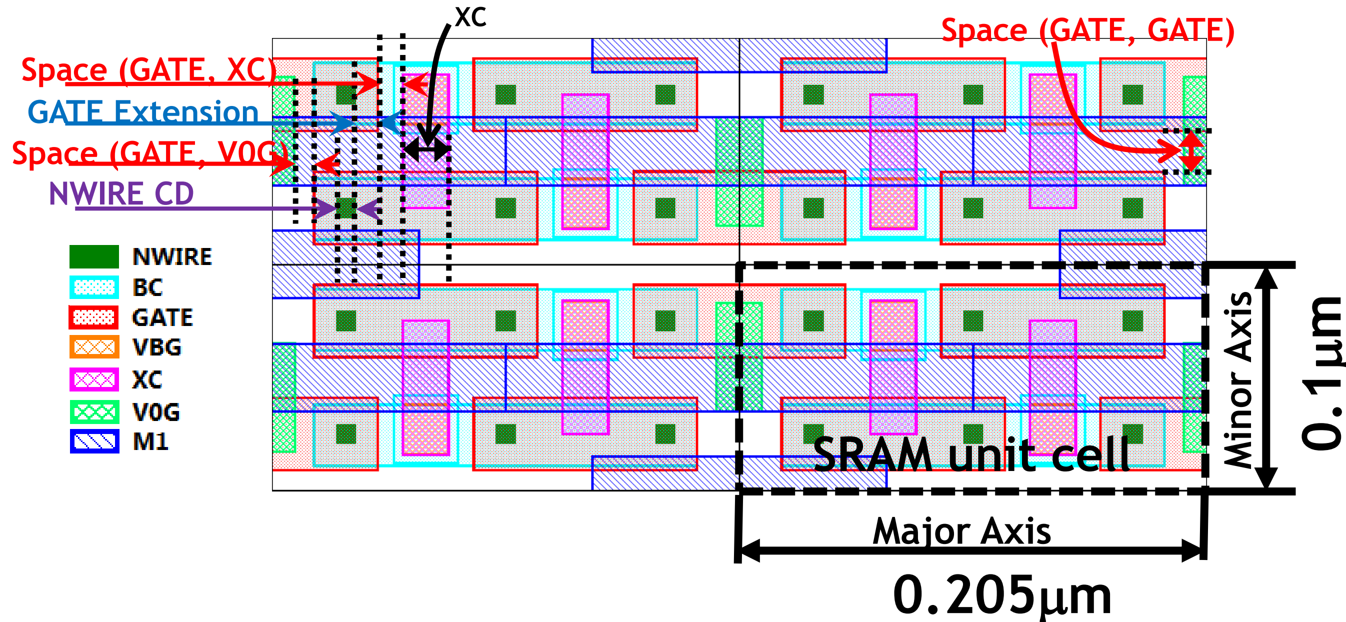
- This work has been supported by Unisantis Electronics via imec-Unisantis Electronics bi-lateral program

- Thanks a lot for your attention!!

- Backup slide hereafter

Design Rule used for the SGT SRAM Test Vehicle

	N14	N10	N7	This work
Poly pitch [nm]	90	66	54	50
Min Metal pitch [nm]	64	44	40	50

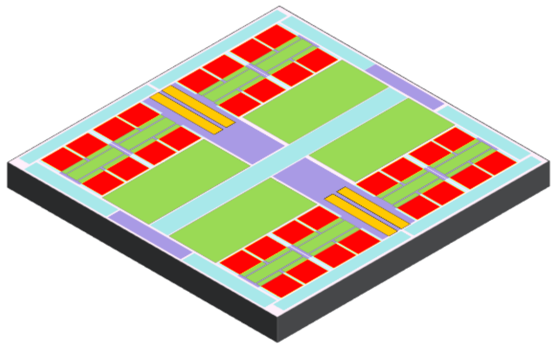


Layer	Description	Pitch(nm)	Wavelength
FEOL Layers			
BPLUS	Bottom Junction	205	193i ArF
NWIRE	Nano-Wire Pillar	50	EUV
BC	Bottom Connection	50	EUV
GATE	Gate Electrode	50	EUV
VBG	Via to BC	54	EUV
XC	X-Couple (GATE-VBG)	70	EUV
NPLUS	NMOS Top S/D	205	193i ArF
PPLUS	PMOS Top S/D	205	193i ArF
MOL Layers			
TE	Top Electrode	70	EUV
TEBLK	Top Electrode Block	100	193i ArF
V0G	Via to Gate	60	EUV
V0T	Via to TE	60	EUV
BEOL Layers			
M1	Metal 1	42	EUV
V1	Via 1	60	EUV
SV1	Super Via1	56	EUV
M2	Metal 2	42	EUV

3D-SOC: Functional partitioning - high performance

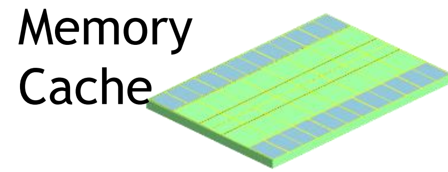
MULTI-CORE PROCESSOR PARTITIONING

2D Multi-core processor

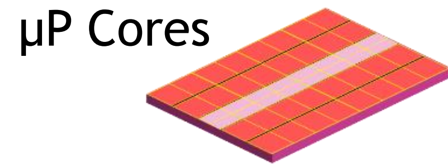


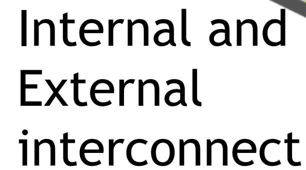
3D functional partitioning

Memory Cache

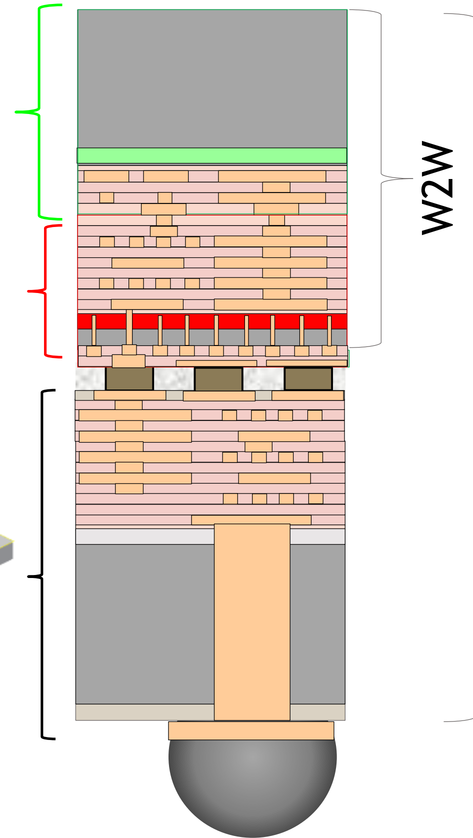


μP Cores





Internal and External interconnect



3D System Integration

SerDes or optical I/O

HBM memory stacks

[Eric Beyne, ITF Future Summit 2019]

Why GEM5 system Simulator?

Runs real workloads

- Runs complex workloads like Android & ChromeOS

System-level insights

- Device interactions (storage, NICs, …)
- OS interactions

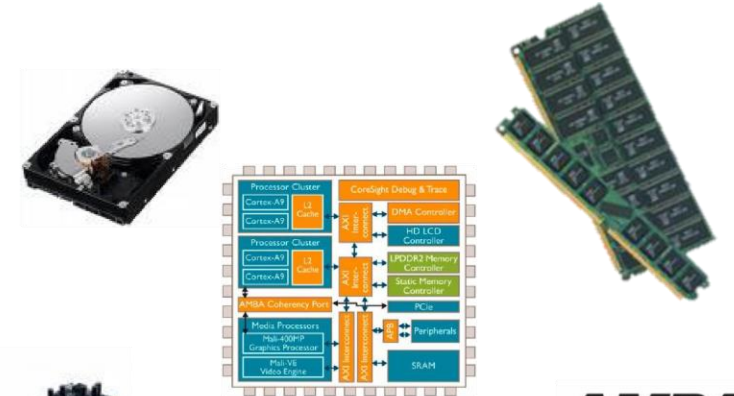
Can be wired to custom models

- *Add detail where it matters, when it matters!*

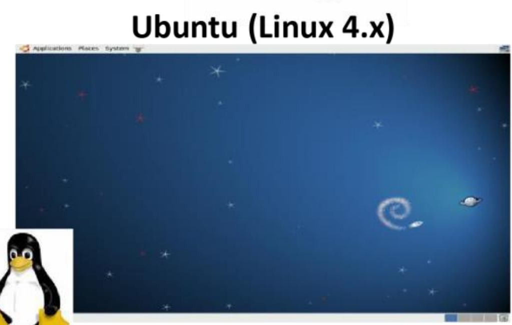
Rapid *early* prototyping

- Parameterized models enable rapid design space exploration

Large user base in industry & academia



Ubuntu (Linux 4.x)

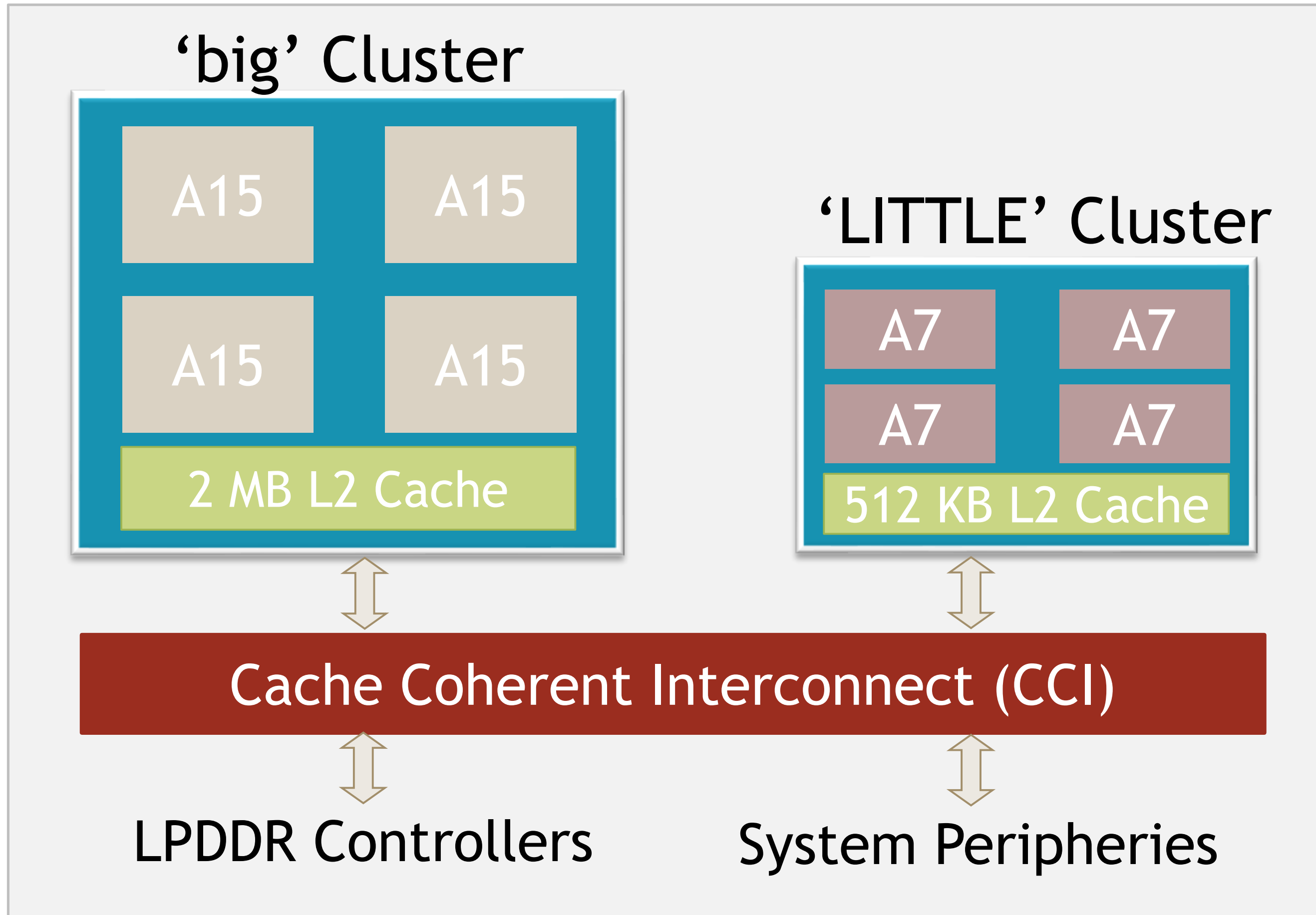


Android Nougat

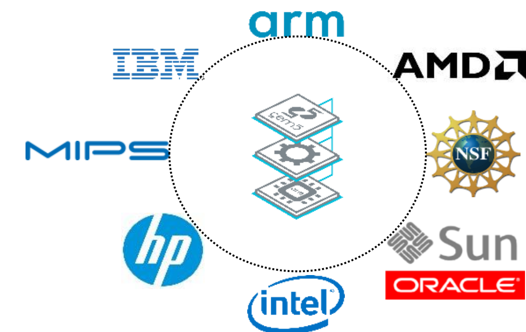
[A.Sandberg, ARM Research]

System level benchmarking with gem5

ARM BIG.LITTLE ARCHITECTURE



- SoC configuration
  - High performance 'big' cluster
    - 4 Cortex-A15 cores
    - 32 KB L1 cache per core
    - 2 MB L2 shared cache
  - Low power 'LITTLE' cluster
    - 4 Cortex-A7 cores
    - 32 KB L1 cache per core
    - 512 KB L2 shared cache
- Similar to Samsung Exynos and Qualcomm Snapdragon 800 series



[T. Huynh-Bao]