12-EUV Layer Surrounding Gate Transistor (SGT) for Vertical 6-T SRAM: 5-nm-class Technology for Ultra-Density Logic Devices

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Abstract

For the first time, we establish a fabrication process flow of an EUV-era ultra-density 6-surrounding-gate-transistor SRAM with 0.0205 μm^2 unit cell area and demonstrate nMOS surrounding-gate-transistor function. In this paper, 6-surrounding-gate-transistor SRAM design layout is shown, and the fabrication process flow and key process steps are explained in detail. NMOS functional device characteristics of surrounding-gate-transistor is analyzed.

Keywords: SGT, GAA, EUV, 6-T SRAM, 5-nm technology, vertical nano-wire

Introduction

Surrounding-gate-transistor (SGT) [1] is a vertical gate-all-around (vGAA) that could make co-integration of density driven volatile and non-volatile memory device [2-4], and high-speed logic devices [5] possible to continue Moore's law beyond 5-nm technology nodes to support the ever increasing demand for more functions per unit area. Some of the authors have conducted a comprehensive benchmark study to compare 6-T SRAM designs using SGT and horizontal GAA (hGAA) bit cells that showed SGT based bit cells can reduce the SRAM area by 20-30% when compared to hGAA based, and that SGT architecture also outperforms hGAA with respect to operating voltage and standby leakage current [6].

In this paper, we show 6-SGT SRAM design layout, and the fabrication process flow complemented by Coventor SEMulator3D™ to experimentally demonstrate that this complex cell can be made.

SGT SRAM Design

The design layout of 2×2 6-SGT SRAM cells, design parameters that govern the unit cell area (width × height), and technology node comparison are shown in Fig.1, Table 1(a), and (b), respectively. A conceptual 3D bird's eye view of 6-SGT SRAM bitcell, and an equivalent 6-T SRAM circuit holding storage data '1' are illustrated in Fig. 2(a) and (b), respectively. We use SRAM cell ratio of 1 : 1 : 1 for pull-up (PU) : pull-down (PD) : pass-gate (PG) SGTs to maximize the packing density. The 6-SGT SRAM unit cell has 0.0205 μm^2 area which makes the SRAM test vehicle in a 5 nm-class technology node (Fig. 3).

Device Fabrication

We used Coventor SEMulator3D™ to explore various process assumptions (PA) before implementing it to silicon. Fig. 4(a) summarizes front-end-of-line (FEOL) to fabricate SGTs, the most disruptive block, and middle-of-line (MOL), back-end-of-line (BEOL) building blocks to wire out SRAM devices.

The FEOL starts with the BPLUS module that creates N+ well by in-situ dope n-type Si epi growth, followed by horizontally abutted N++/P++ well formation via ion implantations (I/I). The top part of this heavily doped wells serves as the bottom source/drain (S/D) extension (Ext.). Activation of the dopant is done by rapid thermal annealing at 1000°C. NWIRE module starts with p-type doped (Si:B) 70-nm channel (Ch.) Si epi growth. The process continues with the formation of 100-nm tall nano-wire (NW) pillars with 8 nm in diameter using single EUV patterning (Fig. 4(b)). A uniform growth of Ch epi thickness which yields uniform NW diameters across P++ and N++ regions is realized by optimizing epi pre-cleaning (Fig. 5). The NW height is higher than the Ch. Si epi layer thickness in order to ensure that the bottom S/D Ext. is in the N++/P++ part of the wells. After the junction and the Ch. formation, we use low temperature (≤ 600°C) processing throughout the remaining process flow, unless stated otherwise. The BC module isolates one set of PU : PD : PG SGTs from the other set of PG:PD:PU SGTs; the two sets constitute the SRAM unit cell (Fig. 4(c)). A typical EUV overlay (OVL) performance between two EUV layers is shown in Fig. 6. The flow then continues with the GATE module to fabricate SGT (Fig. 4(d), (e), and (f)). High-k (HK)/metal-gate (MG)-first scheme consisting of thin chemical oxide as a host interface, atomic layer deposition (ALD) of 1.5-nm thick hafnium dioxide (HfO_2), followed by 3-5 nm thick ALD TiN as a single mid-gap work function metal (WFM), is applied (Fig. 7). After the SGT fabrication, VBG and XC modules follow to strap the SRAM internal nodes between two inverter circuits. VBG contact is one of key components for better SRAM performance, and the Siconi™ removes native oxide under Ti while standard soft sputter etching (SSE) pre-cleaning shows remaining native oxide as analyzed by energy dispersive x-ray spectroscopy (EDS) and electron energy loss spectroscopy (EELS) (Fig. 8). Thus, 10-nm diameter bottom contact with Ti silicide is formed with Siconi™ pre-cleaning. PPLUS/NPLUS top S/D modules complete the SGT by creating top S/D Ext. with heavily doped Si:P selective epi for nMOS and Si:B epi for pMOS.

The MOL block consists of top-electrode (TE), and two via layers connecting the GATE (V0G) and TE (V0T). TE module connects the top S/D with a direct W etch with TECUT + TE litho-etch-litho-etch patterning scheme. The direct W etch approach, where we encapsulate W by a nitride hard mask and a spacer, is beneficial for SGT SRAM as it enables a V0G module with self-aligned-contact etch landing on the GATE that guarantees isolation between the TE and V0G metal layers.

The BEOL block consists of a single damascene M1 module and a dual damascene M2V1 module both with EUV single patterning. A super-via SV module allows direct connection from M2 to TE.

Fig. 9 (a) shows a cross-sectional image of SGT SRAM simulated by Coventor SEMulator3D™ virtual PA. Fig. 9(b) is a transmission electron microscope (TEM) image of fabricated 6-SGT SRAM with the implementation of the virtual PA into real Si. Bottom junction profile design is one of key elements for SRAM function, and P++ and N++ junction profiles along the dashed lines (i) and (ii) shown in Fig. 9 (a) are analyzed by secondary ion mass spectrometry (SIMS) and each impurity profile is shown in Fig. 10 (a), and (b), respectively. Both P++ and N++ region formation by I/I as well as N+ region formation done by *in-situ* doping are confirmed.

Device Characteristics

The experimental validation of the aforementioned process steps is carried out with the use of monitor test structures consisting of multi-dimensional arrays with unipolar SGTs. Fig. 11 shows I_D-V_G characteristics of nMOS device measured at V_D=0.05 and 0.8 V, respectively. Data are from as-drawn NW diameter of 8 nm, physical L_G as-measured by TEM is 21 nm. Subthreshold slope (SS) value at V_D=0.8 V is 125 mV/dec., and threshold voltage (V_{th}) using constant current method is 0.61 V. Our fabricated SGT has potential to be improved by optimization of the fabricated process conditions.

Summary

For the first time, we established the fabrication process of 6-SGT SRAM with 0.0205 μm^2 unit cell area and demonstrated nMOS device function.

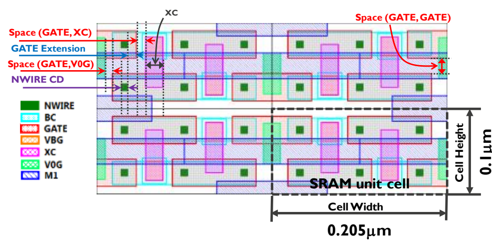

Fig. 1. 6-SGT SRAM design layout with unit cell area of 0.0205 μm^2

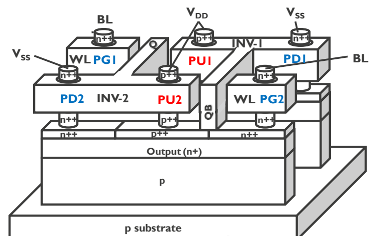

Fig. 2(a). 3D bird's eye view of 6-SGT SRAM unit cell where the storage node 'Q' status is '1'

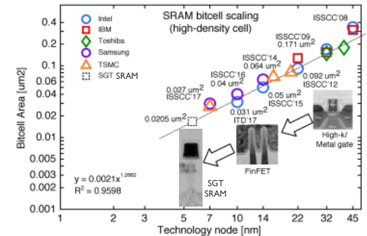

Fig. 3 High-density SRAM area projection and SGT SRAM position at 5-nm-class node.

Table I(a) Cell width, height calculations

	Scaling Sensitive Design Parameters			
Cell width	$3CD_{NW} + 6EXT_{GATE} + 2CD_{XC} + CD_{V0G} + 2SP_{(GATE, V0G)} + 4SP_{(GATE, XC)}$			
Cell height	$2CD_{NW} + 4EXT_{GATE} + 2SP_{(GATE, GATE)}$			
Nominal [nm]	CD_{NW} (x, y)	$Pitch_{NW}$ (x, y)	EXT_{GATE}(x, y)	$SP_{(GATE, XC)}$ (x)
	8, 8	70, 50	10, 12	11

Table I(b) Summary of pitch comparison of this work vs. other technology node

	N14	N10	N7	This Work
Poly Pitch [nm]	90	64	56	50
Min. Metal pitch [nm]	64	48	40	50

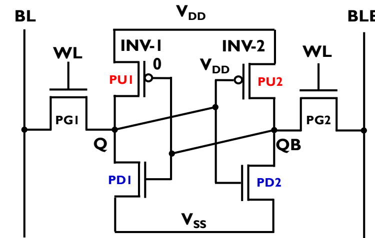

Fig. 2(b). An equivalent SRAM circuit matching to the 3D 6-SGT SRAM view.

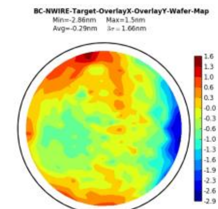

Fig. 6. A typical OVL wafer map between two critical EUV layers (BC and NWIRE). By using the state-of-the-art OVL characterization tools and by applying sophisticated correction algorithms, an OVL value |mean| + 3σ ≤ 3 nm between two EUV layers is achieved.

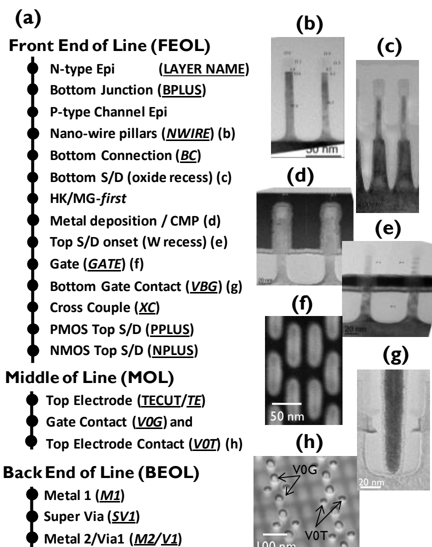

Fig. 4. Modular block flow of (a) FEOL, MOL, and BEOL. Mask layer names are underlined and 12 EUV layers are in italics; FEOL is the most disruptive block (b) to pattern NW pillars, followed by (c) oxide recess, then (d) W CMP, (e) W Recess, and (f) gate patterning; they are key core steps to fabricate SGT. (g) VBG formation and (h) V0G and V0T formation are SRAM specific via modules.

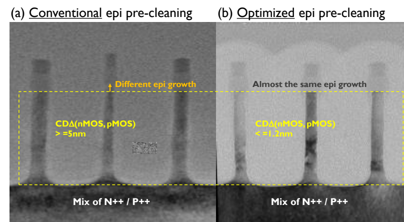

Fig. 5. NW CD delta between nMOS and pMOS after NW etch from (a) conventional epi pre-cleaning (b) optimized epi pre-cleaning.

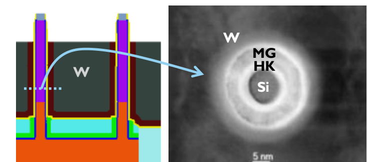

Fig. 7. Coventor SEMulator3D™ intended PA vs. TEM images after Gate W recess where plan view TEM is used to confirm gate stacks.

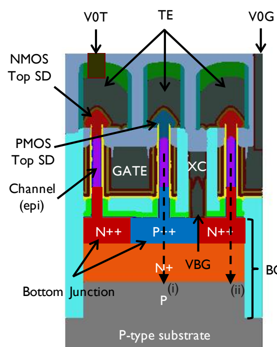

Fig. 9(a). Cross-sectional of 6-SGT SRAM design layout from Coventor SEMulator3D™.

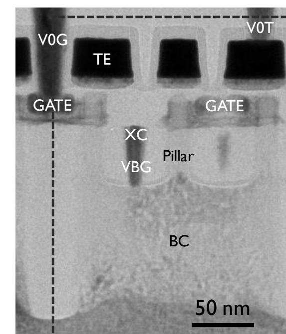

Fig. 9(b). Cross-sectional TEM image of 6-SGT SRAM unit cell (dotted lines) after fully fabricated till M1 module.

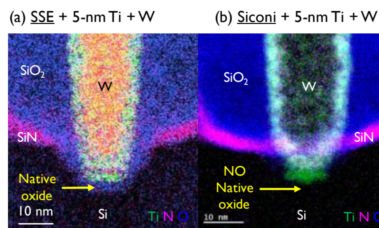

Fig. 8. EDS and EELS analysis after VBG formation with precleaning of (a) SSE, (b) Siconi™.

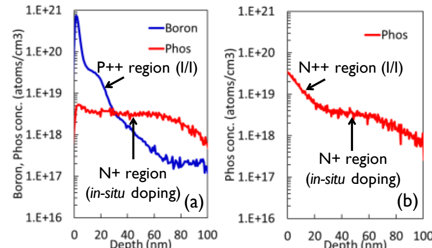

Fig. 10 Impurity profiles of (a) P++ and (b) N++ region along with dashed lines shown in Fig. 8.

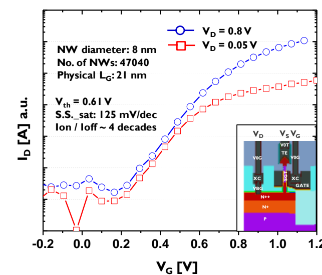

Fig. 11. I_d-V_g characteristics of nMOS device measured at V_d of 0.05 V and 0.8 V. Inset illustrates stand-alone device configuration with SRAM design context.

References [1] H. Takato et al., IEDM Tech. Dig., pp. 222-225 (1988) [2] B. Goebel et al., IEDM Tech. Dig., pp. 275-278 (2002) [3] T. Kikuchi et al., IEDM Tech. Dig., pp. 923-926 (2004) [4] T. Endoh et al., TED, pp. 945-951 (2003) [5] A. Nitayama et al., TED, pp. (1991) [6] T. Huynh-Bao et al., TED, pp. 643-651 (2016)

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