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High Density & Drivability Elongated SGT Transistor for Logic Circuit Having Process Compatibility with 1.5nm node SGT SRAM

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***Abstract*— This paper describes the device structure and manufacturing process of elongated surrounding-gate-transistor (SGT) for the 1.5nm technology node. The elongated layout and self-aligned patternings have successfully realized high density and high drivability for SGT logic. Electrical characteristics by TCAD simulation are demonstrated and discussed.**

Keywords— ***SGT, vertical, nanowire, nanosheet, pillar, Elongated, high density, self-aligned, high drivability***

I. INTRODUCTION

Surrounding-gate-transistor (SGT) SRAM cell for 1.5nm design node was presented in 2021IMW [1]. Continuously, the logic circuit based on the SGT will be discussed in this paper. Circular SGT(CSGT) using circular shape silicon pillar was applied in 1.5 nm node SRAM for the cell size reduction. When multiple CSGTs connected in parallel are used for a logic circuit that requires a high driving current, a wider circuit area is required (Fig.1-a). An elongated SGT (ESGT) can solve this problem because of a feature of smaller area for a high driving circuit (Fig.1-b). Both ESGT and CSGT have been optimally adopted, depending on each circuit requirement with compatible 1.5nm node SGT SRAM process.

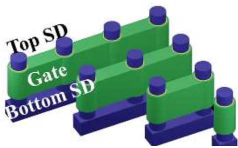

Fig.1-a Circular SGT

Fig.1-b Elongated SGT

II. ELONGATED SGT CHARACTERISTICS

The ESGT characteristics were simulated by using the GTS Nano Devices Simulator (NDS), based on the Kinetic Velocity model [3-4] in order to take the ballistic transport into consideration for large nano scaled device.

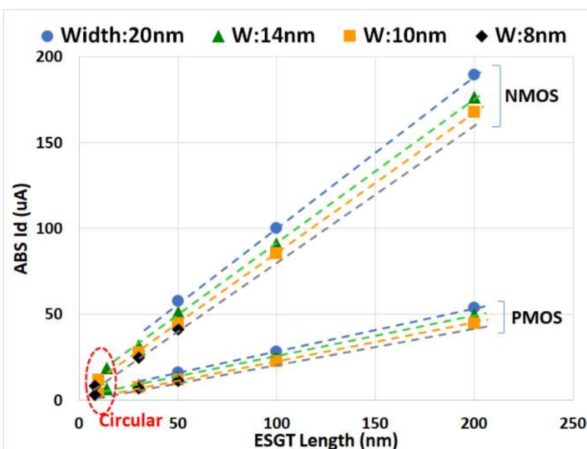

Fig.2 Elongated SGT Length Dependency of Id

Fig. 2 shows drain current can be increased linearly according to elongate length increase. Fig.3-a and -b show the NMOS and PMOS footprint area dependency of drain currents, respectively, which suggest higher drain currents can be obtained by more elongating shape even in the same footprint area. But the PMOS shows this effect is not noticeable compared with the NMOS in the case of less than 100nm elongate length. Conversely, the SS value of ESGT looks a little bit worse than the parallelly connected CSGT.

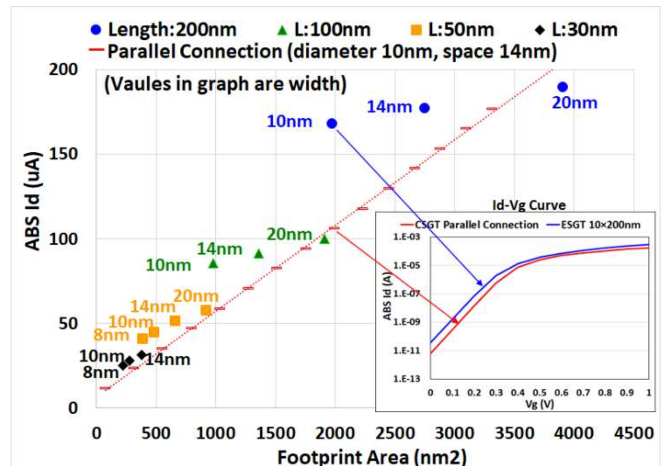

Fig.3-a NMOS Footprint Area Dependency of Id

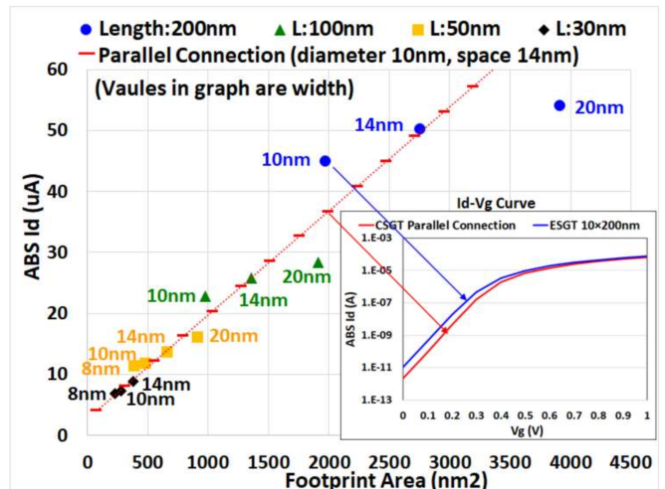

Fig.3-b PMOS Footprint Area Dependency of Id

The SS depends on the pillar width more significantly than the pillar length (Fig.4-a and -b), because the gate can control the narrower pillar more effectively. For example, the SS's of NMOS and PMOS are about 61 and 62 mV/decade, respectively. Decreasing the ESGT width is more effective for suppressing the Ioff without the Ion decrease (Fig.5-a and-

b). Therefore, both the CSGT and ESGT can properly optimize the logic circuit, such as the area, speed and power.

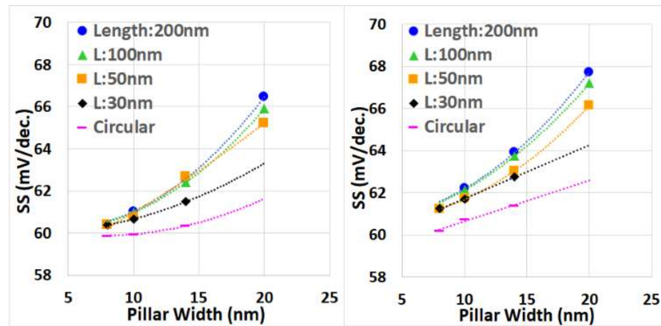

Fig.4-a NMOS Pillar Width Dependency of SS Value

Fig.4-b PMOS Pillar Width Dependency of SS Value

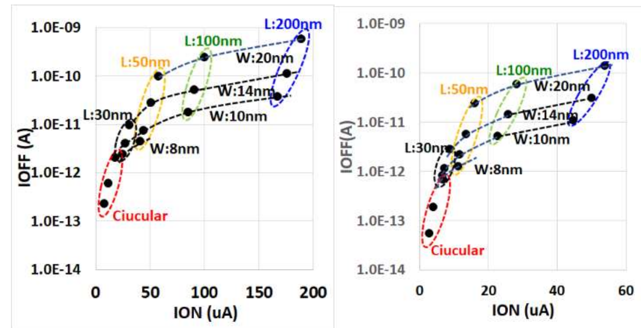

Fig.5-a NMOS SGT ION vs IOFF

Fig.5-b PMOS SGT ION vs IOFF

III. SGT LOGIC LAYOUTs

Fig. 6-a and -b compare the layouts of the invertor circuit for the CSGT and ESGT under the same output current. Area reduction rate can be 62% by using the ESGT.

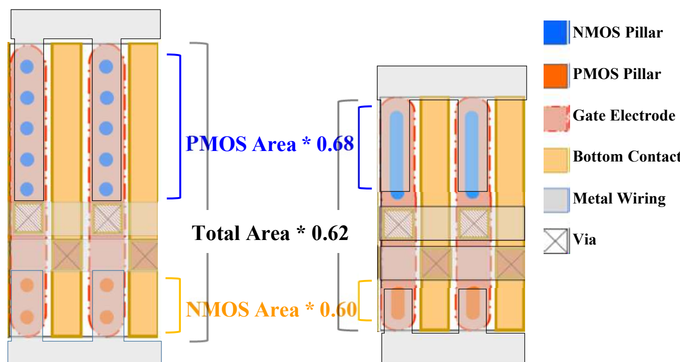

Fig.6-a Invertor using CSGT

Fig.6-b Invertor using ESGT

The combination of the CSGT and ESGT can improve the circuit design. For example, the invertor case needs that the current of NMOS and PMOS should be balanced, so that the CSGT can be used for NMOS, considering from the power consumption. Conversely, in the case of power circuit which needs high drivability, the ESGT NMOS is mainly used without larger footprint area.

IV. MANUFACTURING PROCESS

Elongated SGT process is based on SRAM process for 1.5nm design node with self-aligned process for gate, bottom contact and pillar. Fig. 7 shows the process flow outline and cross section for each process step. Fig. 8, 9 and 10 shows the details of the ESGT process features, such as elongate pillar, gate and bottom contact formation.

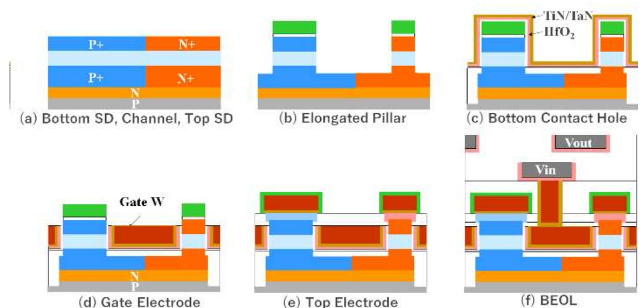

Fig. 7 ESGT Process Cross Section View

(1) Elongate pillar formation

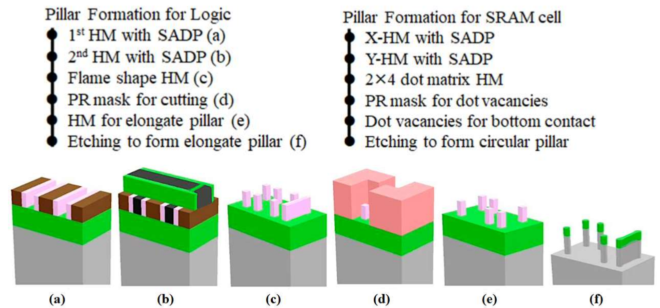

Fig.8 Elongate pillar Formation Flow

Elongate SGT can be easily formed, based on the SRAM circular pillar process.

(2) Bottom Via Formation

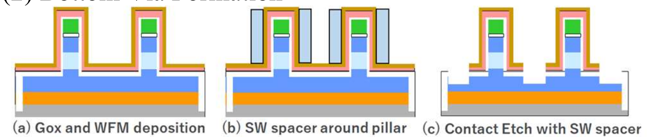

Fig.9 Bottom Via Formation Flow

Bottom contact is formed by self-align to the pillar, which is the same as the bottom contact for SRAM.

(3) Gate Electrode Formation

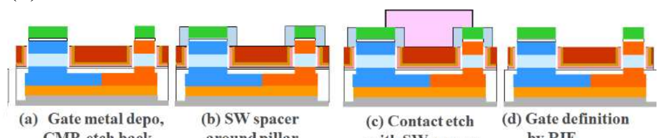

Fig.10 Gate Electrode Formation flow

Gate electrode is formed by self-align to pillar and photo resist, same as the SRAM gate electrode. In this manner, the ESGT process has compatibility with the 1.5nm SRAM cell.

V. CONCLUSIONS

Elongated SGT can get high drivability easily for logic dircuit design with compatibility with the 1.5nm SRAM cell. And logic circuit characteristics can be optimized by using both elongated SGT and circular SGT properly.

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