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Dynamic Flash Memory with Dual Gate Surrounding Gate Transistor (SGT) for Computation In Memory

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***Abstract*—This paper proposes an authoritative architecture for Dynamic Flash Memory (DFM) for Computation In Memory (CIM). With a dual-gate Surrounding Gate Transistor (SGT), a capacitorless $4F^2$ cell had has been proposed earlier [1-2]. Unlike emerging memories with variable resistance, an eigen value current, dependent on the PL voltage, can flow in DFM. Therefore, this characteristic of DFM lends itself to a product-sum operation with low power consumption.**

Keywords—Surrounding Gate Transistor (SGT), GAA, Z-RAM, Capacitorless DRAM, Floating Body, CIM

I. Introduction of the DFM Features

CIM has been studied extensively in emerging memories, such as MRAM and ReRAM. DFM with no variable resistors can flow an eigen value current, which should be a very significant feature for CIM, as it can act as a storage body of the PL gate and a switching transistor of the WL gate. This paper introduces DFM for CIM for the first time.

1. Perfect $4F^2$ Cell Size

Fig. 1 presents the DFM structure, which is composed of single SGT [3] with dual gates. Straight WL's run in the row direction, and straight BL's run in the column direction, so that ultra-scaled $4F^2$ cells exist at their cross-points.

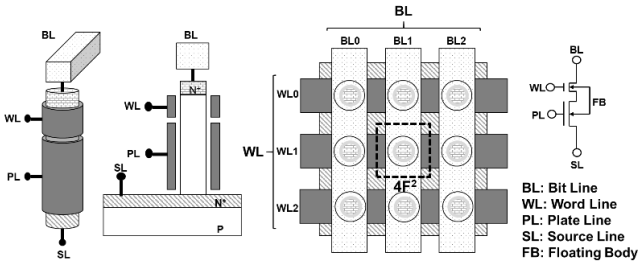

Fig. 1 Standard DFM structure.

2. PL Significantly Reduces WL Capacitive Coupling Ratio

On programming and reading, the PL gate capacitive coupling ratio to the FB (β_{PL}) can significantly reduce the WL capacitive coupling ratio (β_{WL}), as illustrated in Fig. 2.

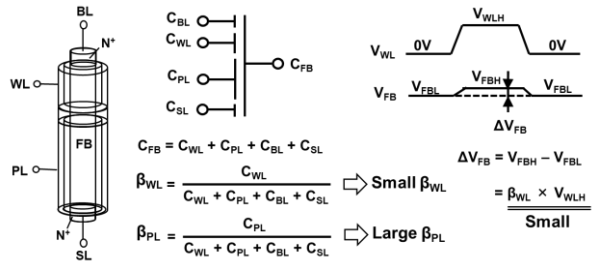

Fig. 2 The FB stabilization by the PL gate.

3. PL Creates Very Large "1"-"0" Margin and Protection

As a certain fixed voltage is applied to the PL gate, the "0" erase threshold voltage of the PL gate can fully prevent flow of the cell current. Basically, the PL and WL gates play a role as a memory device, and a select gate with a variable threshold voltage, respectively. In the case of the "1" program, when generated holes are in the FB, the PL gate can induce a current. The V_{WL} - Icell characteristic shows a saturated eigen value current, which depends on the V_{PL}, as shown in Fig. 3. Conversely, in the "0" erase case, as no holes are in the FB, the PL gate doesn't induce a current. As a result, the PL gate provides a significant "1" and "0" margin. Furthermore, the programmed PL gate can create the inversion layer, so that it can shield the FB from external noises.

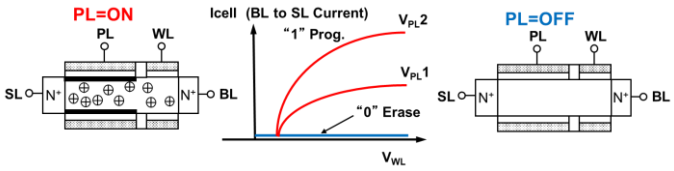

Fig. 3 Wide "1"-"0" margin and the inversion layer shield.

II. DFM Program and Erase Mechanism

1. Programmed by the Source-side Impact Ionization

As for "1" program, the source-side impact ionization will be utilized for the generation of electron-hole pairs, where the PL gate operates the saturation region, while the WL gate operates the linear region with the virtual drain, as shown in Fig. 4. When the WL and BL return to 0V after the generation of holes, they exert little influence on the FB voltage, because the PL gate stabilizes the FB by the large capacitive coupling ratio to the FB (β_{PL}).

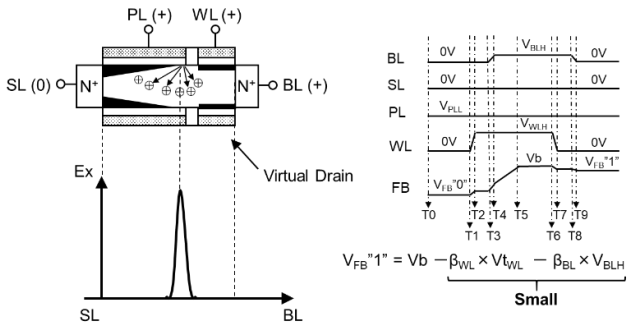

Fig. 4 The DFM "1" program mechanism.

2. Holes push-out erasure by the PL and WL coupling

Fig. 5 presents the holes push-out erasure by the PL and WL capacitive coupling, which requires neither a negative charge pump nor a twin-well process, resulting in a saving in power as well as a reduction in the layout area. In addition, the simple design and fast erasure operation will be attractive. The difference of ΔV_{FB} between the V_{FB}"1" and V_{FB}"0" is sufficiently large, because the sum of the β_{PL} and β_{WL} is close

to 1. Therefore, the wide “0” and “1” margin can be attained without a negative bias circuit.

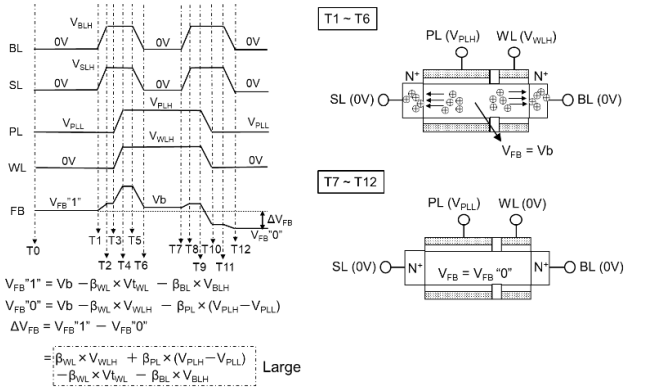

Fig. 5 Holes push-out by the PL and WL coupling to the FB.

III. TCAD Simulation Results

The operation of DFM has been qualitatively validated by T-CAD simulation of by AdvanceSoft Corporation. The model parameters of 1T-DRAM are referred in T. Ohsawa’s paper [4].

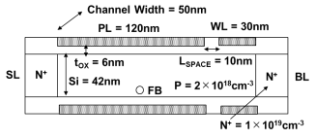

Fig. 6 Simulation model.

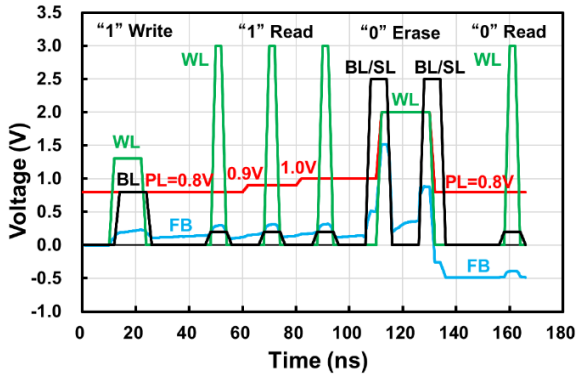

Fig. 7 “1”Write - “1”Read - “0”Erase - “0”Read simulation.

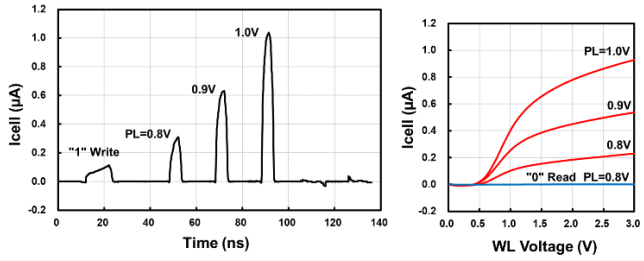

Fig. 8 DFM with an eigen value current for CIM.

Fig. 7 simulates the source-side impact ionization “1” program, three different V_{PL} “1” reads with PL = 0.8, 0.9, 1.0V, holes push-out “0” erasure, and “0” read. Fig. 8 shows its eigen value current. The PL gate operates in the saturation region, while the WL gate operates in the linear region. Therefore, the cell current can be easily controlled by the PL gate voltage. The cell current would represent an eigen value of “1” × 1, “1” × 2, and “1” × 3, by increasing the PL gate voltage, such as PL = 0.8, 0.9, and 1.0V.

IV. Product Sum Operation

Fig. 9 explains the forced inversion type sense amplifier. The reference voltage of VREF controls the T3 current. For example, from a high current to a low current, such as “1” × 2.5, “1” × 1.5, and “1” × 0.5, an eigen value current of “1” × 3, “1” × 2, and “1” × 1 can be obtained. Fig. 10 calculates the product sum operation by the scheme of Multi-Page Selection (MPS). As an example, three pages of data of WL0, WL1, and WL2 are calculated as WL0 × 1 + WL1 × 2 + WL2 × 3, and the result of sums are stored in the Nb_LAT circuit, as a binary number. The MPS scheme can be easily implemented by the address latch circuit in the row decoder.

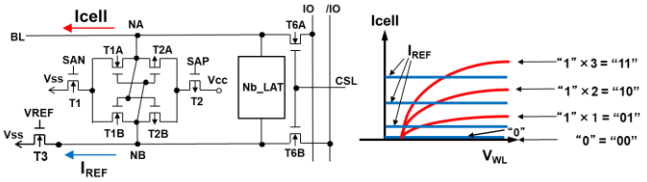

Fig. 9 Forced inversion type sense amplifier.

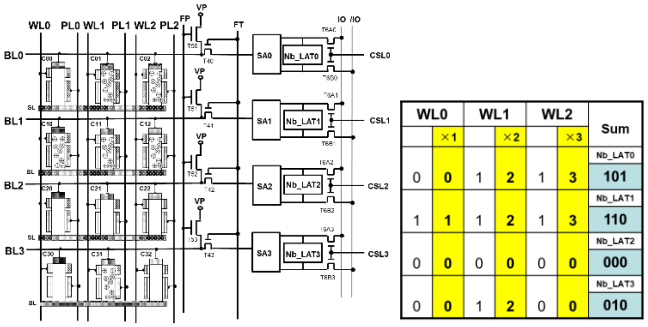

Fig. 10 Product sum operation by the MPS scheme.

V. Conclusions

A definitive architecture for the Dynamic Flash Memory (DFM) has been introduced to enable CIM. An eigen value current, dependent on the PL voltage, can flow through the DFM, which is the most significant requirement for product-sum calculations with a low power operation.

Acknowledgements

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