1.5-nm Node Surrounding Gate Transistor (SGT)-SRAM Cell with Staggered Pillar and Self-Aligned Process for Gate, Bottom Contact, and Pillar

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***Abstract*— We propose the architecture and manufacturing process of 6 surrounding-gate-transistor (SGT) SRAM cell for the 1.5nm technology node. The staggered layout and self-aligned patternings have successfully realized a transition from 5nm to 1.5nm node with the same SGT diameter. Electrical characteristics by TCAD simulation are finally demonstrated.**

Keywords— ***SGT, surrounding gate transistor, vertical, nanowire, pillar, SRAM, high density, self-aligned***

I. INTRODUCTION

Slowdown of Moore's Law, where the transistor count doubles every generation transition, has been being a serious issue not only for stand-alone memory chips but also for SoCs, which inevitably include SRAM. V. Moroz et al. highlighted the issue that SRAM scaling in a post-planar era is slower than logic scaling [1]. According to their analysis, the scaling factor for SRAM remains in a range between 1.1 and 1.3 after 10nm node, while the transistor density for logic circuitry increases by a factor between 1.4 and 2.0 at a technology node transition.

For the post-FinFET era from or after 3nm node, a number of three-dimensional structures have been proposed, such as horizontal Gate-All-Around (GAA) nanosheet [2], Complementary FET (CFET) [3], and a p-channel nanoribbon FET on an n-channel FinFET [4]. All these architectures employ a gate fully surrounding a channel of the transistor for the best electrostatic control. We had presented the paper on the 5nm node SRAM at the 2019 Symp. VLSI Technology, "Surrounding Gate Transistor (SGT) based SRAM cell technology for 5nm node" [5]. The SGT uses a vertical cylindrical pillar as the channel body with current flowing vertically.

In this paper, we introduce a single-storied SGT-based 6T-SRAM cell for 1.5nm node with a scaling factor of 1.40 per node, as shown in Fig. 1. Key enablers of this SRAM cell are 1) a staggered pillar arrangement, 2) footprint minimized gate, and 3) bottom contact for cross-coupling by self-aligned patterning with sidewall spacers formed around pillars. This aggressive scaling achieves a single-storied structure without stacking transistors, which are prevalent in horizontal GAA devices.

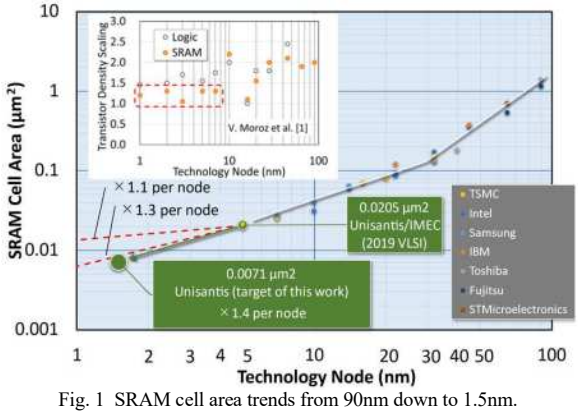
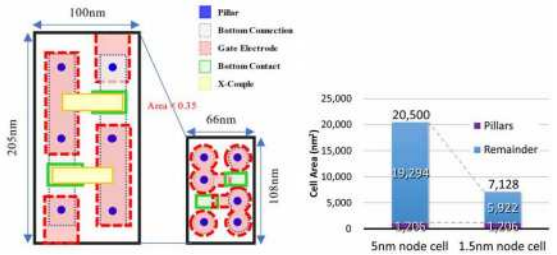


Fig. 1 SRAM cell area trends from 90nm down to 1.5nm.

II. 1.5NM SRAM CELL DESIGN

The 1.5nm SRAM cell area of 0.0071μm² (Fig. 2 (a)) with a scaling factor of 1.40 per node is achieved, in comparison with the 5nm cell area of 0.0205μm². This great leap has passed through two intermediate nodes of 3nm and 2nm nodes. The shrinkage is performed with the same pillar diameter of 8nm (Fig. 2 (b)). The ultra-scaled area has been successfully achieved by tightening design rules of only few layers, such as a pillar spacing, clearances of bottom contacts for cross-couplings, and bottom source/drain connection sizes of storage nodes from the 5nm cell. These tightenings, however, do not impose a significant burden on the lithography.



(a) Layout comparisons (b) Footprint comparisons

Fig. 2 Plan views and cell footprint comparisons of SGT SRAM cells.

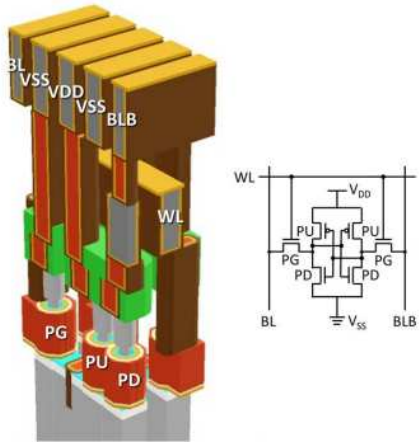


Fig. 3 Bird's eye view of 1.5nm SRAM cell.

The cell structure is shown in Fig. 3. Cross-coupling wiring of the cell is embedded just under the lower edge of the surrounding gate. The word-line (WL) runs as Metal-1 and V_{DD}, V_{SS}, bit-line (BL), and bit-line bar (BLB) run as Metal-2.

III. Manufacturing Process

A. Outline

Fig. 4 shows an outline of the process flow. Six pillars are fabricated through epitaxial growth of doped layers ((a), (b)), orthogonal SADP, and culling pillars. Bottom contact holes for cross-coupling of the cell are made between the WFM deposition step and the gate metal deposition step (c). Metal, such as tungsten, is deposited, planarized, and etched back to form gate electrodes and cross-coupling wiring at the same time (d). Terminals of doped silicon are epitaxially grown on source/drain of the SGTs (e). BEOL then follows (f).

B.

- Silicon substrate
- Bottom S/D, channel, and top S/D layers by epitaxial growth (a)
- Staggered pillars (b)
- Bottom contact holes for cross-coupling (c)
- Gate electrodes (d)
- Top source/drain electrode (e)
- followed by BEOL (f)

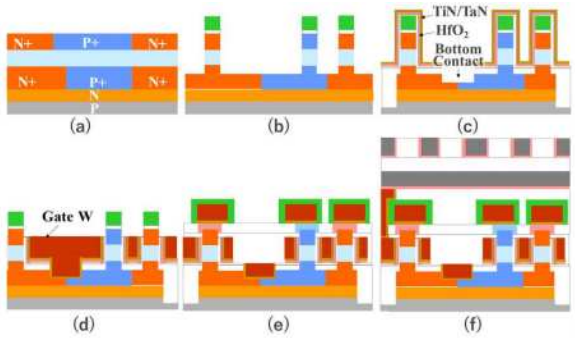


Fig. 4 Outline of manufacturing process.

- X-directional hard mask with SADP spacers (a)
- Y-directional hard mask with SADP spacers (b)
- 2 × 4 dot matrix hard mask (c)
- Photoresist mask for dot vacancies (d)
- Dot vacancies generated for cross-coupling spaces (e)
- Controlled etching to form silicon pillars (f)

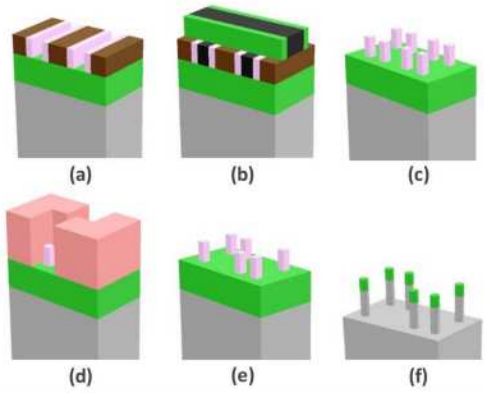
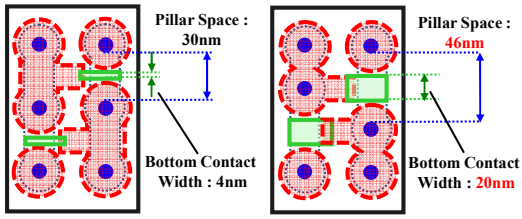


Fig. 5 Staggered pillar arrangement flow.

Fig. 5 illustrates the process flow of the staggered pillar formation. A hard mask film to form a 2×4 dot matrix in a cell area is defined by an orthogonal self-aligned double patterning (SADP) with EUV lithography [6, 7] ((a), (b), (c)). Two vacancies for spaces to form cross-coupling of storage nodes are made by removing hard mask dots by subsequent lithography and etching steps ((d), (e)). The staggered six pillars are then formed by RIE (f).

A bottom contact for a mirror symmetric layout becomes too narrow (4nm) to form an electrically stable contact. By adopting the staggered pillar arrangement, a five-fold larger contact width (20nm) compared to a mirror-symmetric layout can be successfully achieved (Fig. 6), and consequently, manufacturability of the contact is secured.



(a) Mirror symmetric layout (b) Staggered layout

Fig. 6 Mirror-symmetric layout vs staggered layout.

C. Bottom Contact of Cross-coupling Self-aligned to Pillar

The bottom contact formation flow is shown in Fig. 7. High-k dielectric and work-function metal (WFM) films are deposited to cover sidewalls of the pillars by CVD (a). A dielectric, such as a silicon dioxide film, is deposited and anisotropically etched to form sidewall spacers around pillars. A bottom contact hole is formed by etching with sidewall spacer masks. The bottom contact formation, prior to gate definition, effectively avoids short-circuiting between the cross-coupling contact and gate.

- HIgh-k dielectric and WFM deposition (a)
- Sidewall spacer formation around pillars (b)
- Bottom contact by etching with sidewall spacer masks (c)

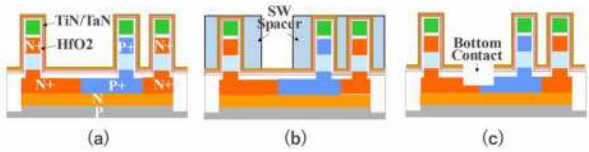


Fig. 7 Bottom contact formation flow for cross-coupling.

D. Gate Self-aligned to Pillar

The gate formation flow is shown in Fig. 8. After barrier metal and contact metal films are deposited and then planarized by CMP, they are etched back to form the bottom contact. A gate metal film is deposited by CVD and planarized by CMP. The gate metal and the work-function metal are etched back down to the design height of the upper edge of the gate (a). A dielectric film is deposited and etched back to form sidewall spacers around pillars. Tips of the pillars have been capped with another dielectric film after the pillar definition. As tips of the pillars have been capped with another dielectric film since the pillar definition, all the surface of parts of pillars exposed above the level of the gate metal surface, including their tips and sidewalls are now covered with dielectrics (b). Photoresist masks for gate extensions are defined by EUV lithography (c). The gate is formed by RIE, using the dielectrics and the photoresists as etching masks. The main cylinder part of the gate, besides its extension, is defined in a self-aligned manner with the sidewall spacer. Therefore, the gate length is decoupled from the cell footprint (d).

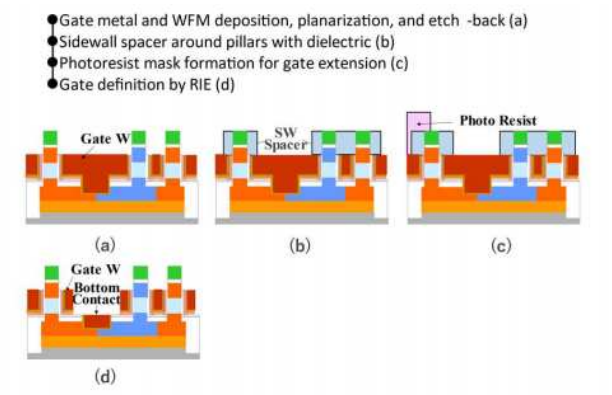
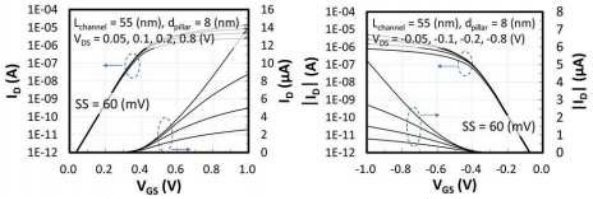


Fig. 8 Self-aligned gate formation flow.

IV. SINGLE SGT CHARACTERISTICS

A. I_D-V_{DS} Characteristics by TCAD Simulation.

Transistor characteristics of SGT-nFET and pFET were simulated by using the GTS Nano Device Simulator (NDS), based on the Sub-band Boltzmann Transport Equation [8]. Both have the same channel length of 55nm, defined by a distance of metallurgical p-n junctions at source and drain edges, and the same pillar diameter of 8nm. I_D-V_{GS} characteristics are shown in Fig. 9. Both nFET and pFET showed an ideally low subthreshold slope of 60mV/dec. and proved that the structure of SGT has superior electrostatic control.



(a) nFET (b) pFET

Fig. 9 I_D-V_{GS} characteristics of SGTs.

B. Short-channel Effects

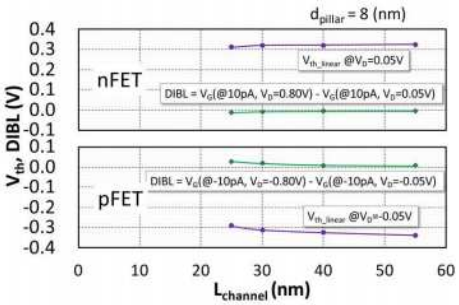


Fig. 10 Threshold voltage roll-off and DIBL characteristics.

Threshold voltage roll-offs and drain induced barrier lowering (DIBL) are shown in Fig. 10. DIBLs between $|V_{DS}|$ = 0.05V and 0.80V. As for the threshold voltage roll-offs of the 55nm channel length nFET and pFET, they are 5mV and 6mV, respectively. Those of the 25nm channel length nFET and pFET are 14mV and 27mV, respectively. While short-channel effects are effectively suppressed, a channel length of SGTs for the 1.5nm SRAM cell is chosen to be 55nm just for safety.

C. Pillar Diameter Effects

A drain current per effective channel width, *i.e.* a perimeter of a cylinder of the pillar of SGT ($\pi\, d_{pillar}$), is

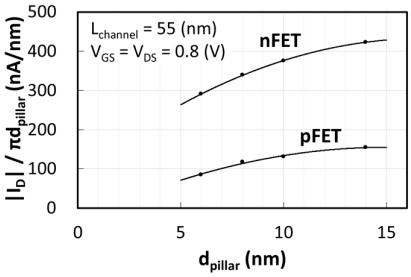


Fig. 11 Pillar diameter dependency of unit current drivability.

dependent on the pillar diameter as shown in Fig. 11. The unit drain current deteriorates as the diameter decreases.

The increase in resistance occurs in the channel itself. There are two mechanisms which drive the current deterioration:

1. The quantum confinement in the channel repels electrons from the Si/SiO_2-interface. In narrower channels, the inversion density is reduced by this effect, and so is the current.
2. All carrier scattering is enhanced in narrow channels, but most notably surface roughness scattering. Carrier scattering reduces mobility, and thus carrier velocity, and ultimately current.

As for circuit performances including SRAM operations, there two challenges we have; 1) the pillar diameter should not be shrunk proportionally to the whole cell, but by a certain shrinking rate, or 2) no change in the diameter should be made.

V. 6-SGT SRAM CHARACTERISTICS

A. Static Noise Margins

6-SGT SRAM characteristics were investigated by using the GTS Cell Designer (CD), which provided detailed circuit and parasitic analysis in 3D [9]. Butterfly curves of the 5nm and 1.5nm cells are almost identical, and stability of operation of the 1.5nm cell is preserved through the cell size shrinkage (Fig. 12).

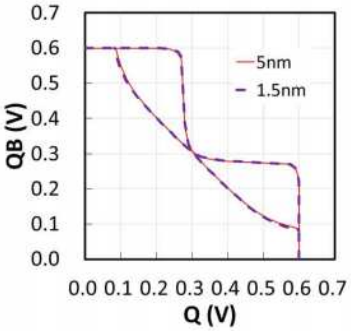


Fig. 12 Butterfly curves of 5nm cell and 1.5nm cell.

Read static noise margins (RSNMs) larger than 100mV are secured down to 0.5V of power supply (Fig. 13). This result is consistent to a trend of SRAM for commercially available SoCs of advanced technology [10].

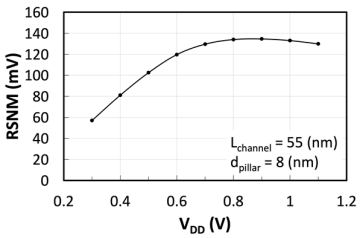
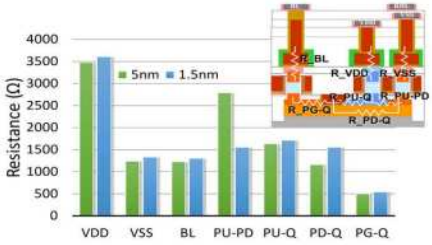


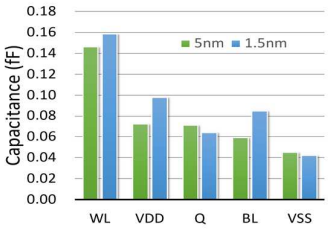
Fig. 13 Read static noise margins (RSNMs) as a function of V_{DD}.

B. SRAM performances

Parasitic resistances and capacitances of SRAM cell were analyzed in comparison with the 5nm cell. Primary resistances such as R_{VDD}, R_{VSS}, R_{BL}, $R_{PU\text{-}PD}$, $R_{PU\text{-}Q}$, $R_{PD\text{-}Q}$, and $R_{PG\text{-}Q}$ are shown in Fig. 14 (a). They do not show significant changes except for a resistance between drains of PU and PD, $R_{PU\text{-}PD}$. The reduction is due to the pillar pitch shrinkage, thanks to the orthogonal SADP. Conversely, capacitances shown in Fig. 14 (b) slightly increase due to shorter distances between nodes, while maintaining the same size of the pillars.



(a) Parasitic resistances



(b) Parasitic capacitances

Fig. 14 Parasitic resistances and capacitances of SRAM cell.

Fig. 15 simulates the write operation. Despite the increase of parasitic capacitances, adverse effects on read and write operations were found to be very limited. A write delay from the WL for 1.5 nm was 92 ps, which was an increase of only 5% from 88 ps of the 5nm case.

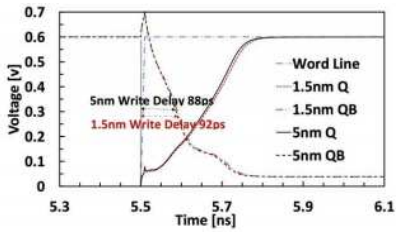


Fig. 15 Write operations of SRAM.

VI. Conclusions

The architecture and manufacturing process of an ultra-scaled SRAM cell with six SGTs at 1.5nm node were presented, and the electrical characteristics of the device were demonstrated through TCAD. A staggered arrangement of pillars for SGTs and multiple use of self-aligned patterning with sidewall spacers around pillars require no significant tightening of design rules of critical layers in a transition of technology nodes from 5nm to 1.5nm. The pillar diameter was maintained, so that transistor's current drivability is preserved. The utility of self-aligned patterning is one of the most advantageous characteristics of vertical SGTs, which horizontal devices, such as horizontal GAA nanosheet FETs, do not have. A high feasibility of achieving the cell area of $0.0071\mu m^2$ was finally demonstrated. Through the achievements, single-storied SGT technology was demonstrated to make the most promising candidate for the 1.5nm node and beyond, as shown in Fig. 16. As for next step, we continue the studies on the SGT pillar pitch scaling.

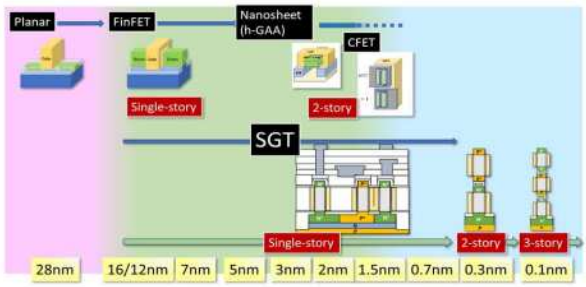


Fig. 16 Technology Roadmap.

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