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2 bit/cell Dynamic Flash Memory with Three Gates

Koji Sakui, Yisuo Li, Yoshihisa Iwata, Masakazu Kakumu, and Nozomu Harada
Unisantis Electronics Singapore Pte Ltd., 60 Paya Lebar Road, #10-49 Paya Lebar Square, Singapore 409051
sakui@unisantis.com

***Abstract*—This paper proposes the Muti-Level (2 bit/cell) Dynamic Flash Memory (MLC DFM) with three gates for realizing a long retention time. MLC DFM has been validated by Silvaco TCAD simulation. The four-level retention time achieves 100 ms at 85 °C.**

Keywords—DFM, Surrounding Gate Transistor (SGT), GAA, Capacitorless DRAM, 1T-DRAM, Floating Body, SOI, FinFET

I. Introduction of the DFM Features

The biggest motivation of the research on the DFM is that DRAM has only made modest gains in scaling over the years of its use and development. An attempt to reduce the cell size from $6F^2$ to $4F^2$ has been thwarted by numerous difficulties, such as the three-dimensional capacitive couplings, as well as the need of a high aspect ratio cell capacitor to store certain charges. The capacitorless 1-transistor DRAM (1T-DRAM) has been studied extensively over the last 30 years [1-3]. However, the issue of the *WL-FB* (Word Line - Floating Body) capacitive coupling prevented commercialization. With respect to utilizing a bipolar action, a certain current flow is needed for holding a stable state [4]. We have studied these issues, and have presented the DFM [5-12]. In this paper, the 3G_DFM, which has a long hole retention time, and robust disturbance shield as a superior device, has proposed the 2 bit/cell DFM for realizing a low bit cost DFM.

II. 3G_DFM Features

1. *3G_DFM Structure*

Fig. 1 illustrates the 3G_DFM structure, which is composed of a single SGT [13] with triple gates of *SG1*, *PL*, and *SG2*. Straight Page's run in the row direction, and straight *BL*'s run in the column direction, so that ultra-scaled $4F^2$ cells exist in their cross-points.

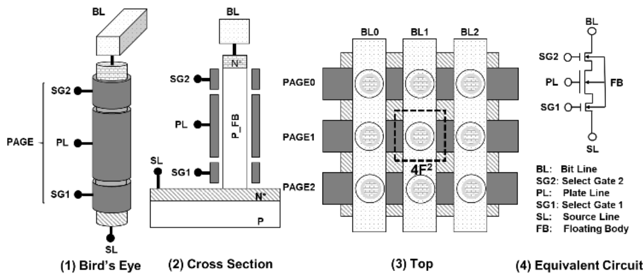

Fig. 1 The 3G_DFM structure built by SGT.

Two select gates of *SG1* and *SG2* can electrically shield the *FB* from the disturbance noise of the *BL* (Bit Line) and *SL* (Source Line), so that the retention time of the stored holes under the *PL* (Plate Line) is extended, as shown in Fig. 2.

2. *Programmed by the Source-side Impact Ionization*

For the "1" program, the source-side impact ionization will lead to the generation of hole-electron pairs. During the "1" program the *PL* and *SG2* gates operate in the linear region with the virtual drain of the inversion layer beneath *PL* and *SG2*, while the *SG1* gate operates in the saturation region. For example, V_{SG1} = 1.2V, V_{PL} = 1.5V, V_{SG2} = 1.5V for the selected page, while 0V is applied to all the other gates for the unselected pages, as shown in Fig. 3. The random data of "1" are programmed to the selected cells after the page erasure. The *BL*'s are applied with from 0.7V to 1.0V, dependent on the MLC data. As the *Cell_01* in Fig. 3 should be suffered from the disturbance during programming, the *SG2* can protect the *FB* from the *BL* noise. Also, the electric field, which causes the *GIDL* (Gate Induced Drain Leakage) current, is relatively lower than that of 1T-DRAM, because it requires to apply the negative voltage, such as -1.5V, for the unselected *WL*'s.

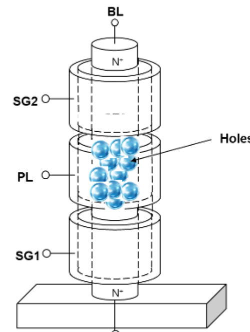

Fig. 2 Robust structure.

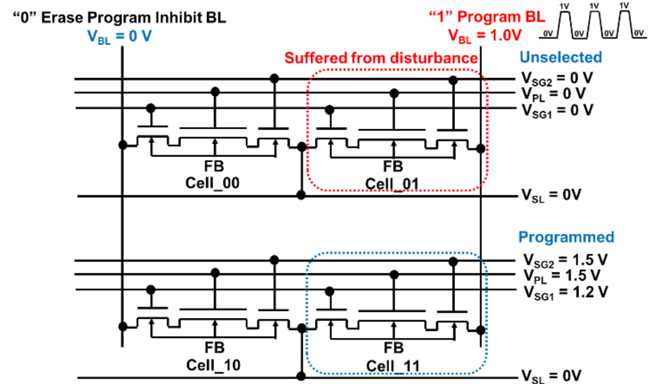

Fig. 3 Memory cell array architecture.

3. *Erased by the Positive Voltages of PL and SG2*

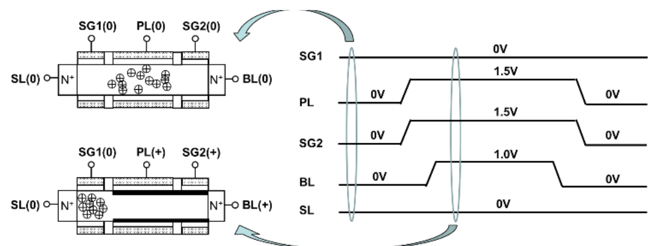

Fig. 4 "0" Erased by the positive voltages of *PL*, *SG2*, and *BL*.

Unlike 1T-DRAM, no negative voltage is applied to the *BL* or *SL* in the case of the holes push-out erasure, as shown in Fig. 4. As a result, neither a negative charge pump nor twin-well process is needed, so that not only the power but also the layout area will be reduced. Furthermore, the simple design and fast erasure operation will be attractive and promising.

III. TCAD Simulation Results

1. *TCAD Simulation Model for the 3G_DFM*

The operation of the 3G_DFM, as shown in Fig. 5, has been qualitatively validated by Silvaco 2D T-CAD simulation.

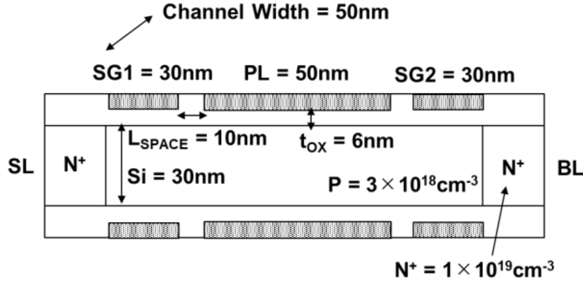

Fig. 5 The simulation model parameters of the 3G_DFM.

2. *2 bit/cell Simulation Results*

The 4-level 3G_DFM has successfully achieved a wide margin of “11”, “10”, “01”, “00”, as shown in Fig. 6. The 2 bit/cell DFM can be sensed by increasing the *PL* voltage of V_{PL} from 0.6V to 1.0V on reading, as shown in Fig. 7. For example, at V_{PL} = 0.7V, “11” can be sensed and latched into the 2 bit flip-flops. Then, at V_{PL} = 0.8V, “10” can be sensed, and so forth.

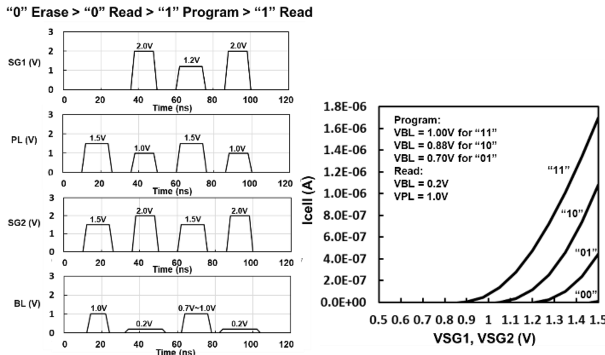

Fig. 6 The 2 bit/cell 3G_DFM standard operation.

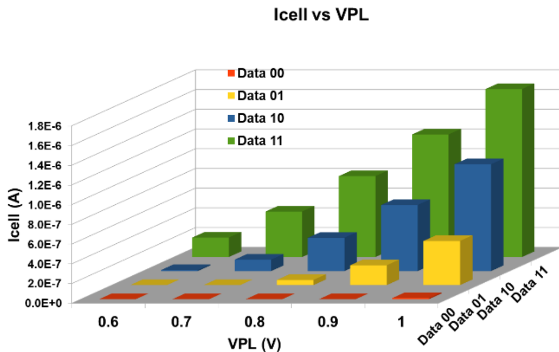

Fig. 7 The 2 bit/cell is read by increasing V_{PL} voltages.

The 4-level retention time has achieved 100 ms at 85°C. Each read plot was simulated one by one, so as not to accumulate the regenerated holes by the read operation. Two select gates of *SG1* and *SG2* can shield the disturbance noise of the *BL* and *SL*.

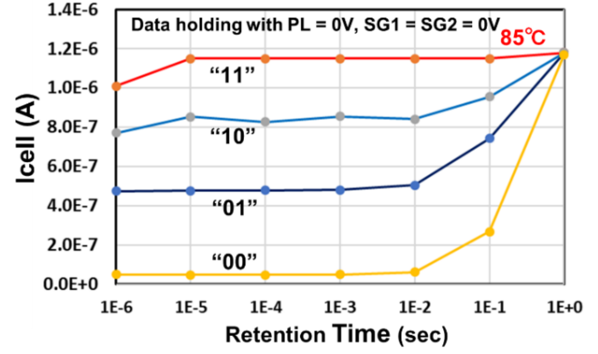

Fig. 8 The 2 bit/cell retention time simulation result at 85°C.

IV. Conclusion

The 2 bit/cell 3G_DFM can be successfully validated with the retention time of 100 ms at 85 °C by virtue of the *SG1* and *SG2* shield for the *FB* disturbance. It should be noted that the MLC DFM is promising to provide a low bit cost memory.

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