ssdm2023
Sponsored by
2023 International Conference on Solid State Devices and Materials

Poster Session Date and Time: 15:00 - 17:00 on 7 September
Area: 02: Advanced and Emerging Memories / New Applications Room 234 (Bldg. 2)

2 bit/cell Dynamic Flash Memory with Three Gates

Koji Sakui, Yisuo Li, Yoshihisa Iwata, Masakazu Kakumu, and Nozomu Harada

Unisantis Electronics Singapore,
60 Paya Lebar Road, #10-49, Paya Lebar Square, Singapore
409051 sakui@unisantis.com

UNISANTIS ELECTRONICS

Semiconductor Memories

DRAM: R. H. Dennard, "Field-Effect Transistor Memory," *U.S.P. 3,387,286*, Filed on Jul. 14, 1967.

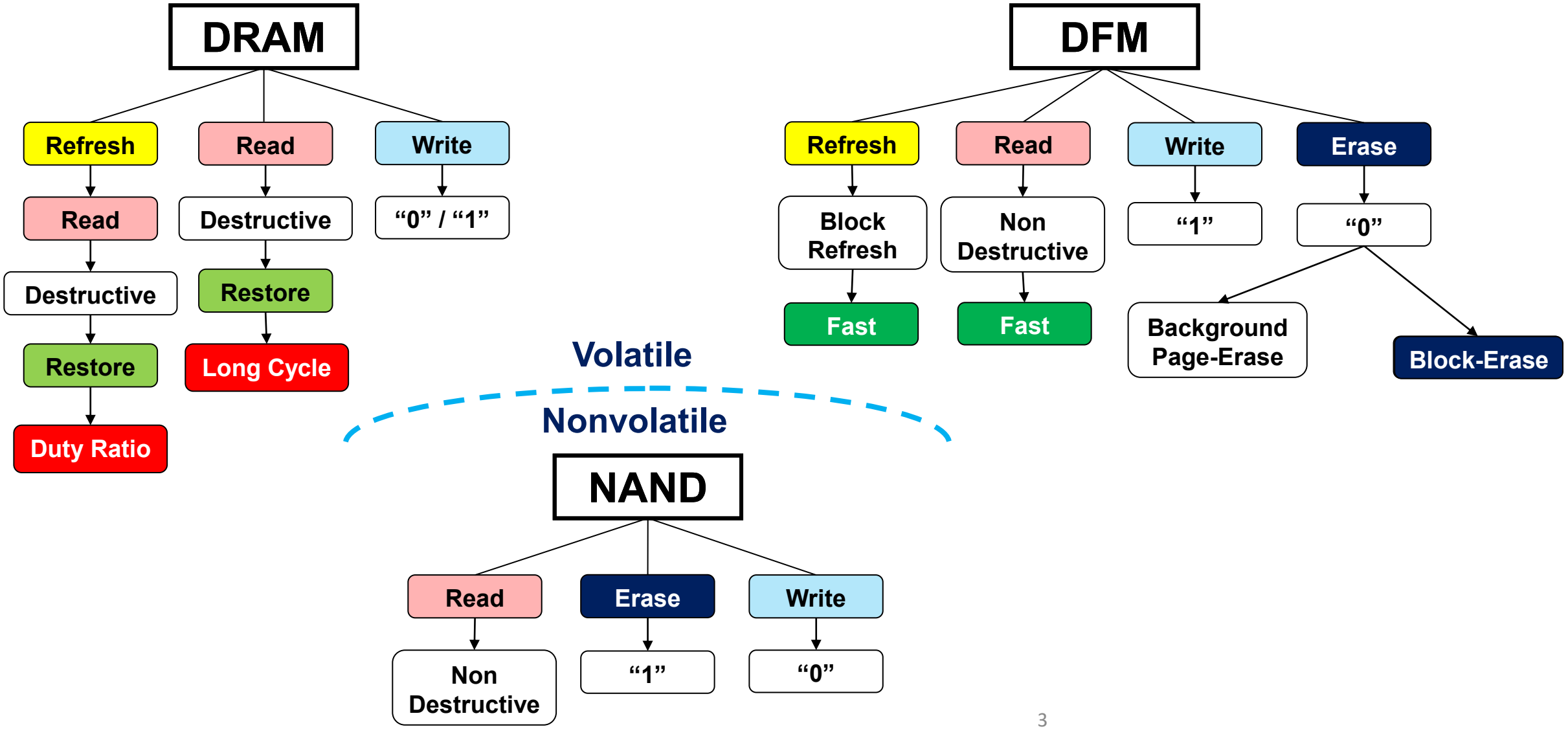
Flash: F. Masuoka, "Semiconductor Memory Device," *U.S.P. 4,437,174*, Filed on Jan. 19, 1981 (Japan)..

An enormous number of ideas have been emerged after DRAM and Flash.

Questions are

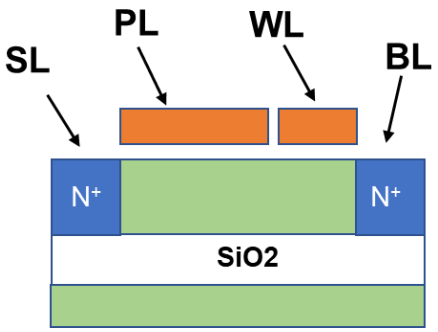
1. What is the key specification of emerging memories in comparison with DRAM and NAND?
    1. Cost
    2. Speed
    3. Power
    4. Any others
2. What is the merit of using different materials from the conventional Si process?

DFM Concept

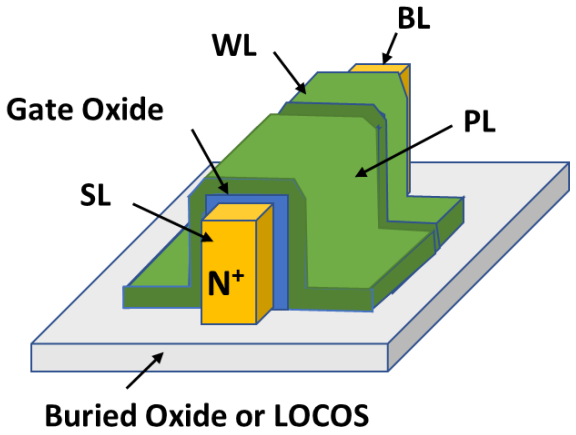


3

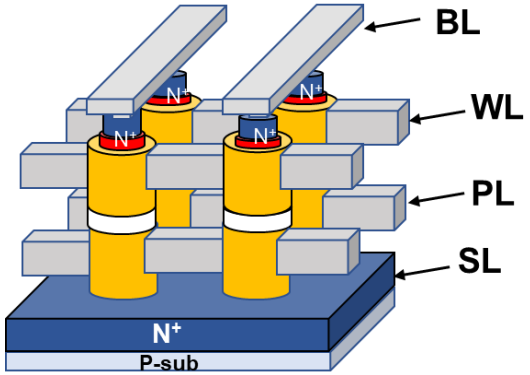
DFM Structure



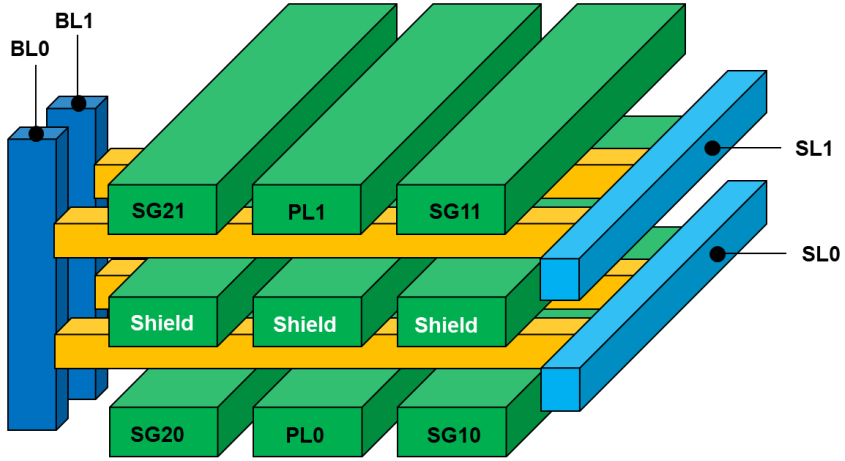
(1) SOI DFM



(2) FinFET DFM

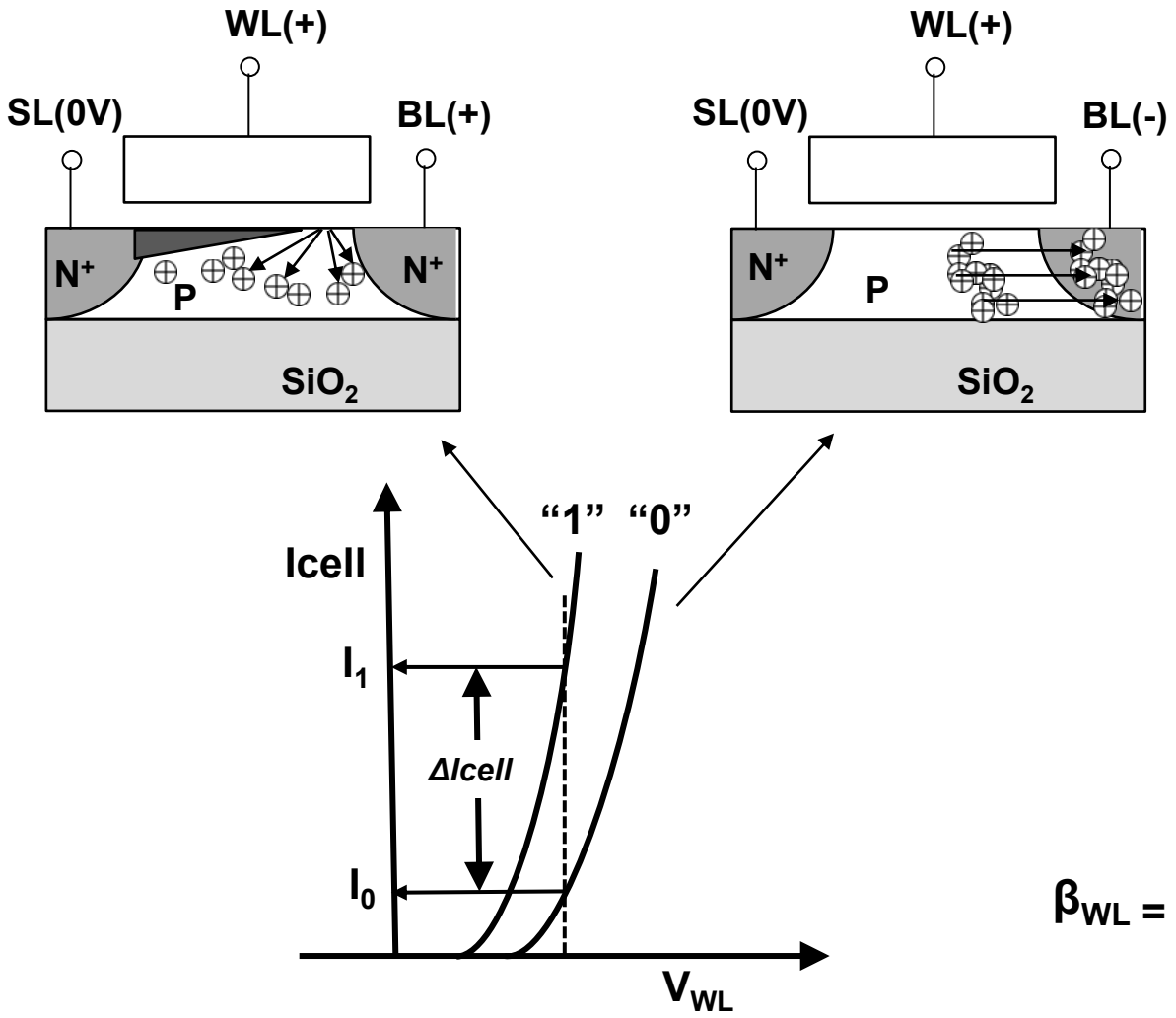


(3) SGT DFM



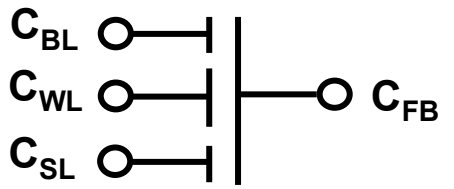
(4) Stack DFM

1T-DRAM (Z-RAM)

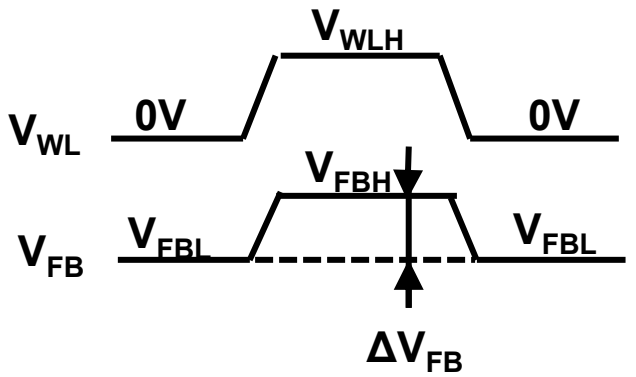


Concerning

1. Large WL capacitive coupling to FB
2. Small "1" and "0" margin
   1. Cell Vth is defined by WL
   2. Negative WL is required for maintaining "1"



$$C_{FB} = C_{WL} + C_{BL} + C_{SL}$$



$$\beta_{WL} = \frac{C_{WL}}{C_{WL} + C_{BL} + C_{SL}} \Rightarrow \text{Large } \beta_{WL}$$

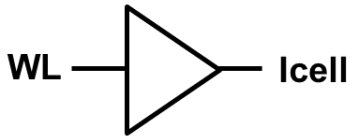
$$\Delta V_{FB} = V_{FBH} - V_{FBL}$$

$$= \frac{\beta_{WL} \times V_{WLH}}{\text{Large}}$$

K. Sakui, "Semiconductor Storage Device," *Japanese Patent Application* Number: 01-311386, Publication Number: 03-171768, Filed on Nov. 30, 1989.

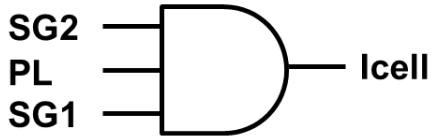
Wide “1”-“0” Margin

Logical Expression



WL	Icell
1	1
0	0

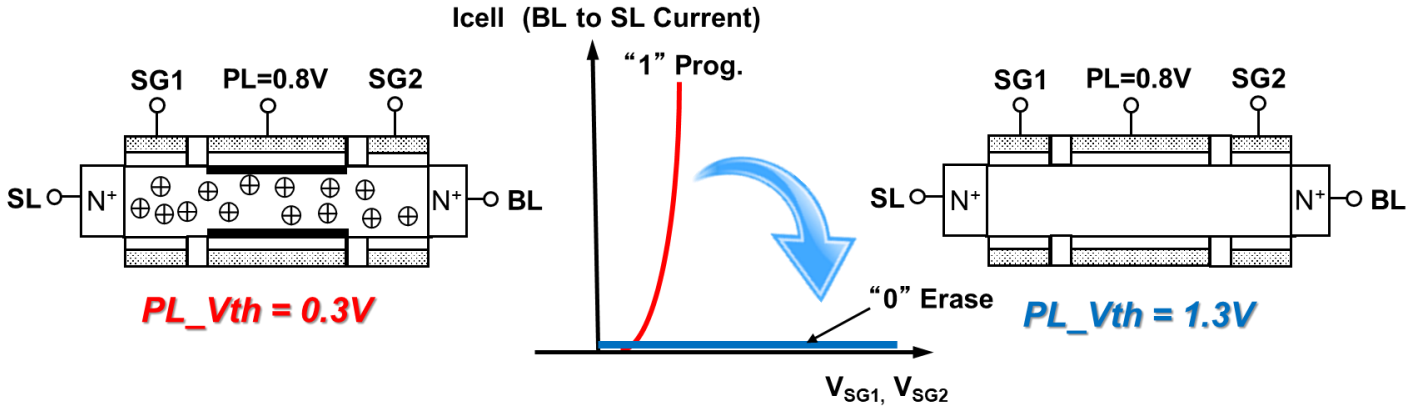
(a) 1T-DRAM



SG1	PL	SG2	Icell
1	1	1	1
1	1	0	0
1	0	1	0
1	0	0	0
0	1	1	0
0	1	0	0
0	0	1	0
0	0	0	0

(b) 3G_DFM

PL plays a storage, while SG1/SG2 plays a switch !



A fixed voltage of 0.8V is applied to PL on reading.

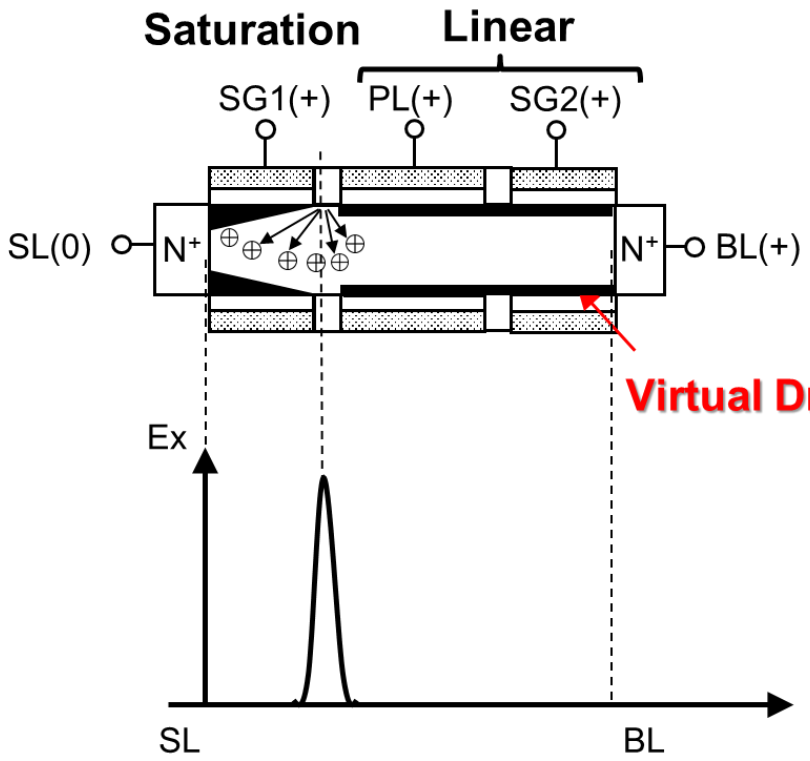
K. Sakui, Y. Li, M. Kakumu, K. Kanazawa, I. Kunishima, Y. Iwata, and N. Harada, “Design Impact on Three Gate Dynamic Flash Memory (3G_DFM) for Long Hole Retention Time and Robust Disturbance Shield,” in *Memories - Materials, Devices, Circuits and Systems, Elsevier*, 4, 100054, pp.1-5, May 2023.

“1” Program and “0” Erase Mechanism

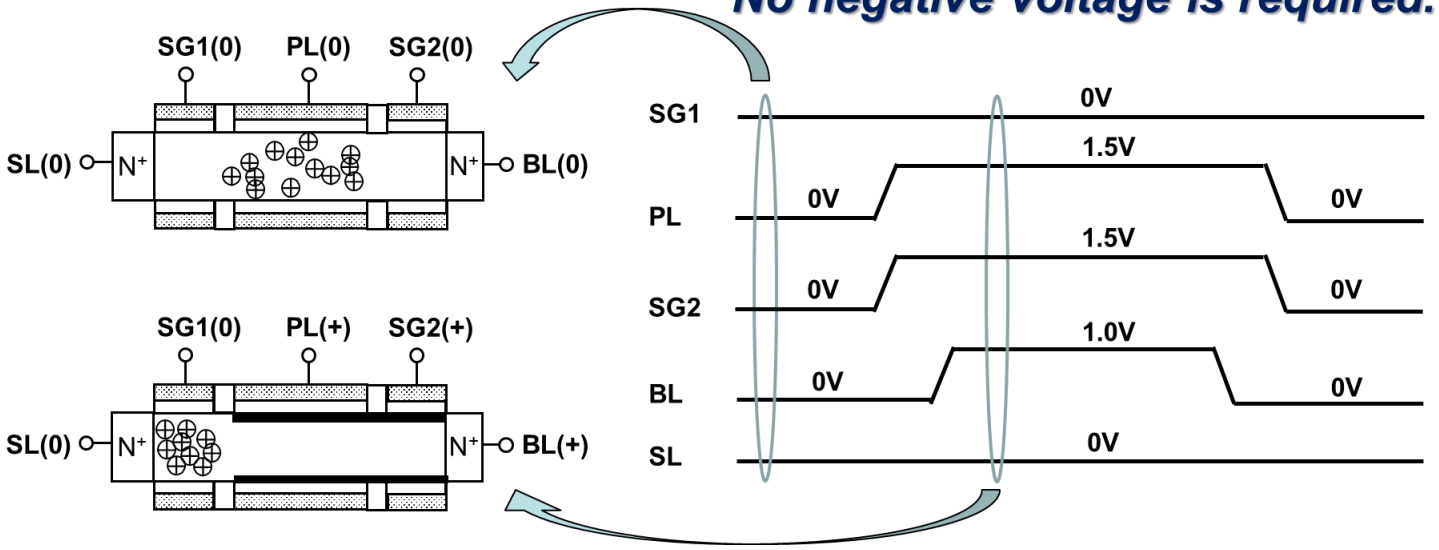
“1” Program

“0” Erase

~Source-side Impact Ionization~

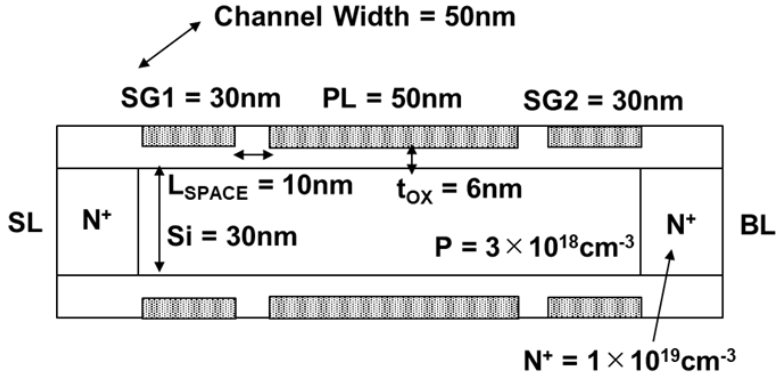


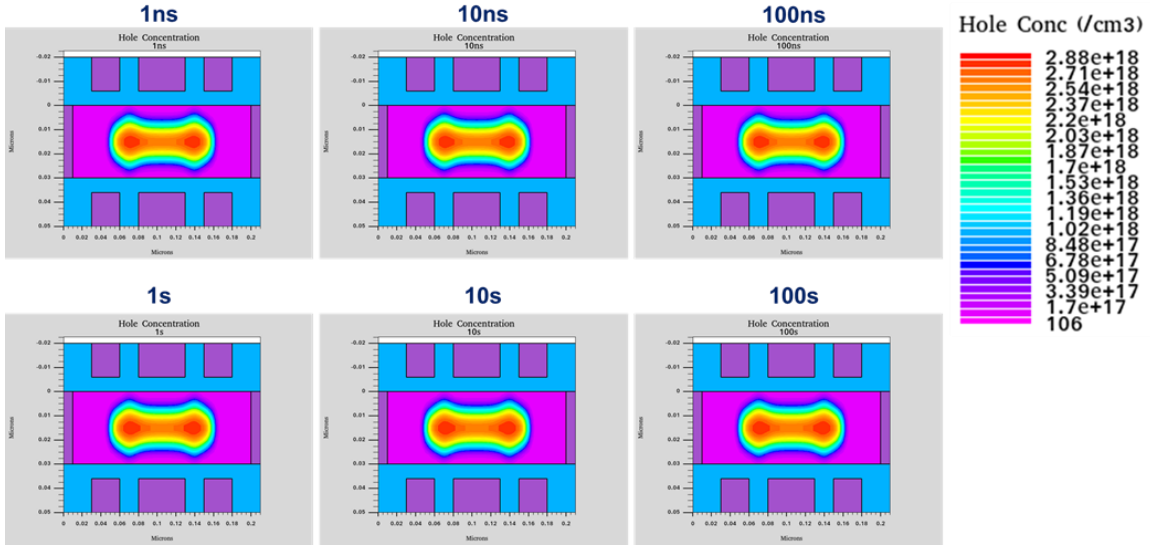
No negative voltage is required.

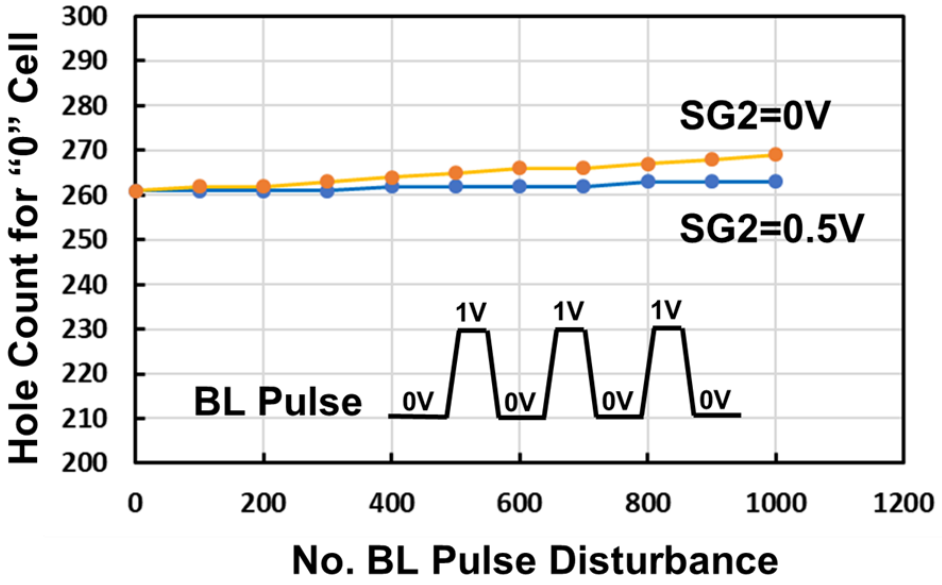


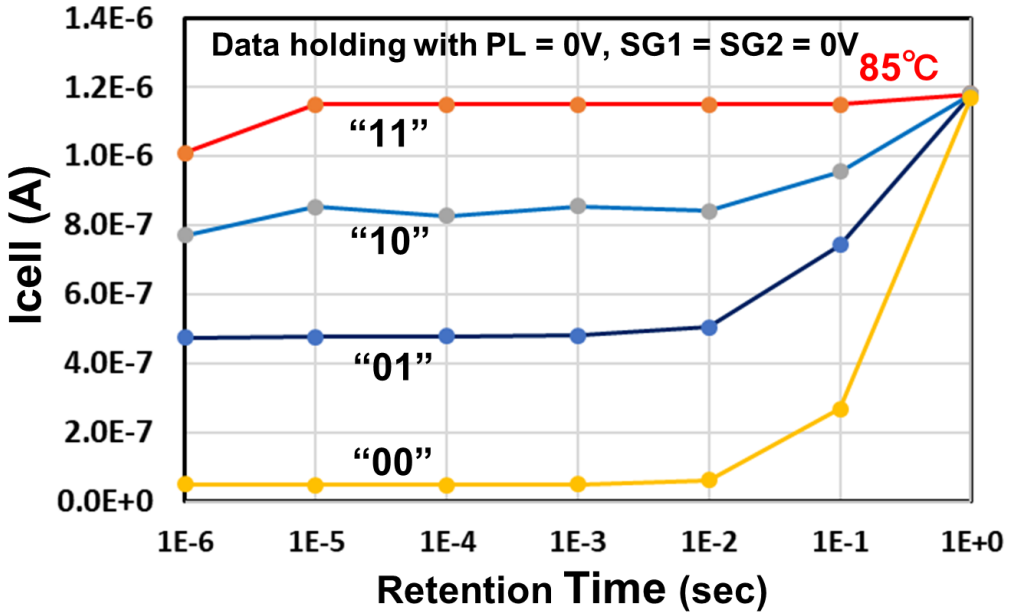
K. Sakui, Y. Li, M. Kakumu, K. Kanazawa, I. Kunishima, Y. Iwata, and N. Harada, “Design Impact on Three Gate Dynamic Flash Memory (3G_DFM) for Long Hole Retention Time and Robust Disturbance Shield,” in *Memories - Materials, Devices, Circuits and Systems, Elsevier*, 4, 100054, pp.1-5, May 2023.

2 bit/cell 3G DFM Retention and Cycling

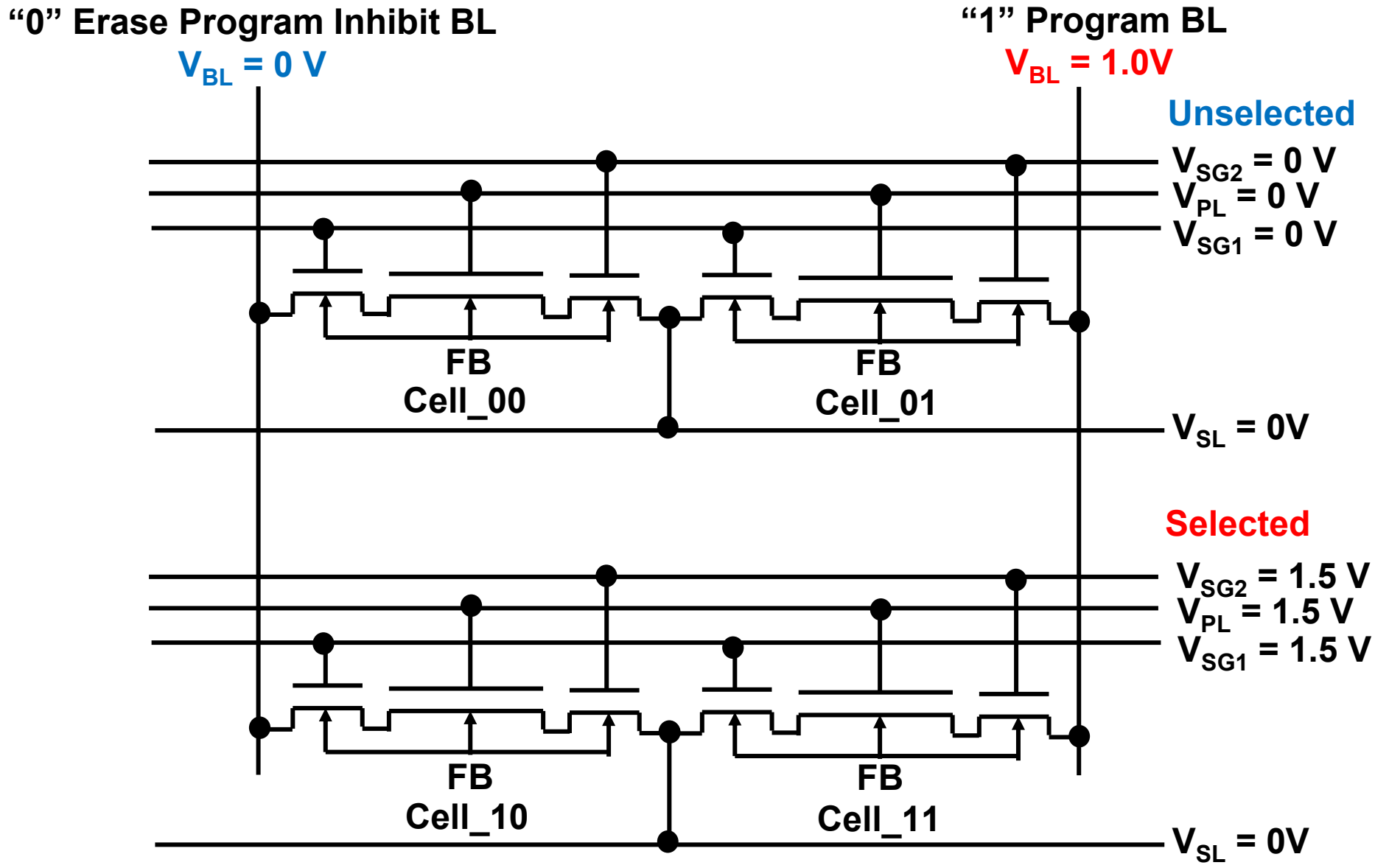






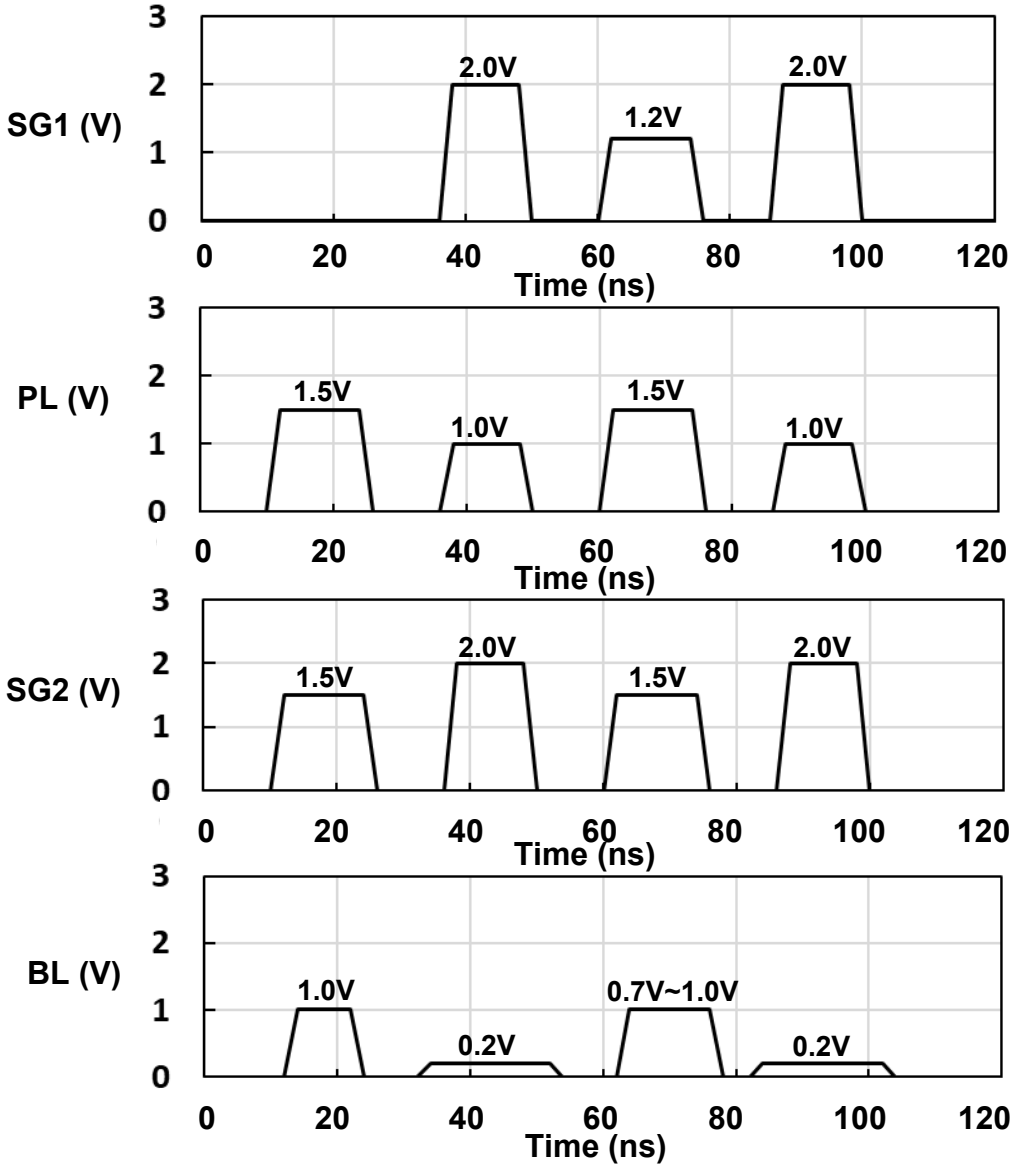


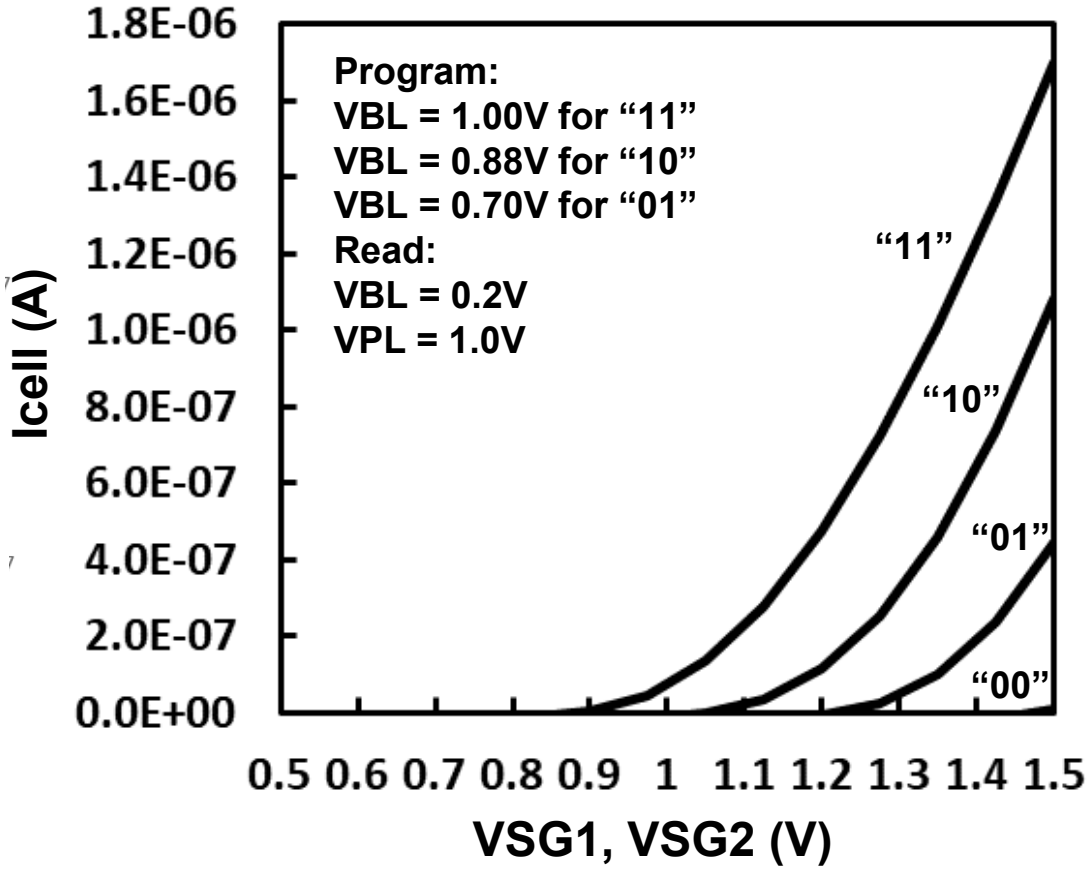
Robust Disturbance



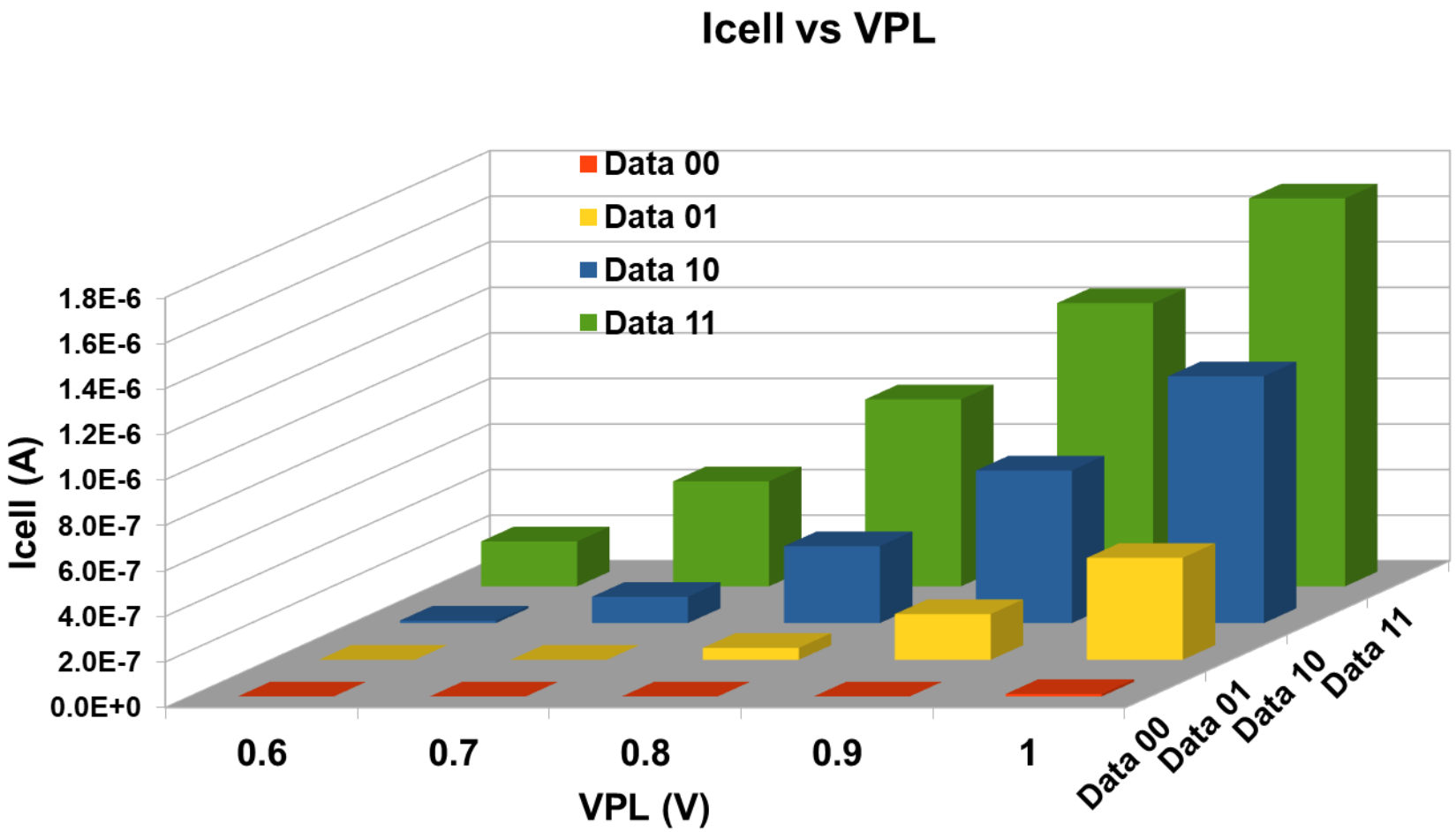
2 bit/cell 3G DFM Standard Operation

“0” Erase > “0” Read > “1” Program > “1” Read





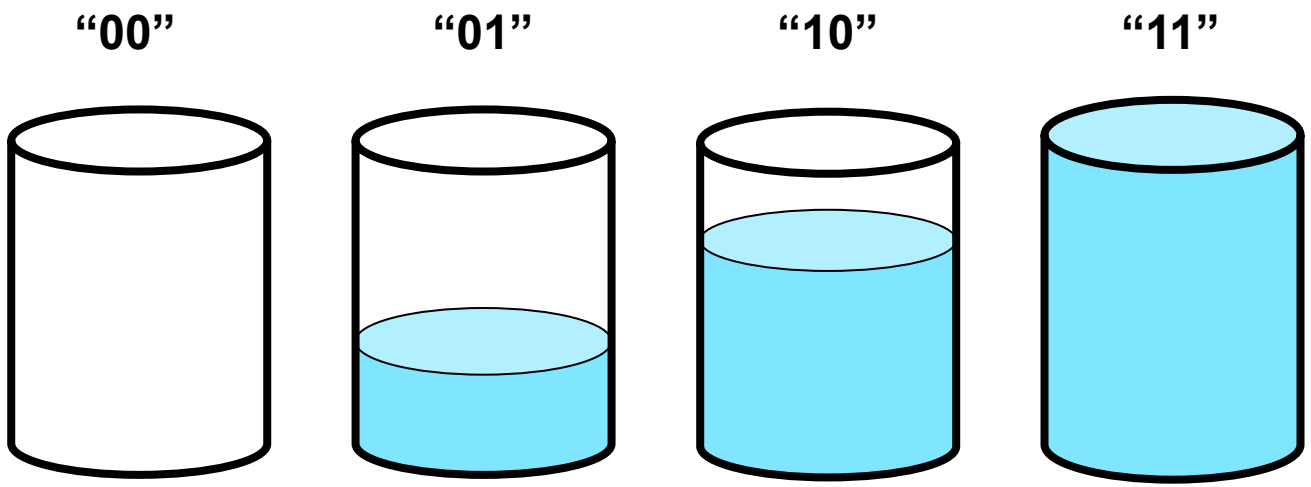
2 bit/cell Read by increasing *VPL* voltages



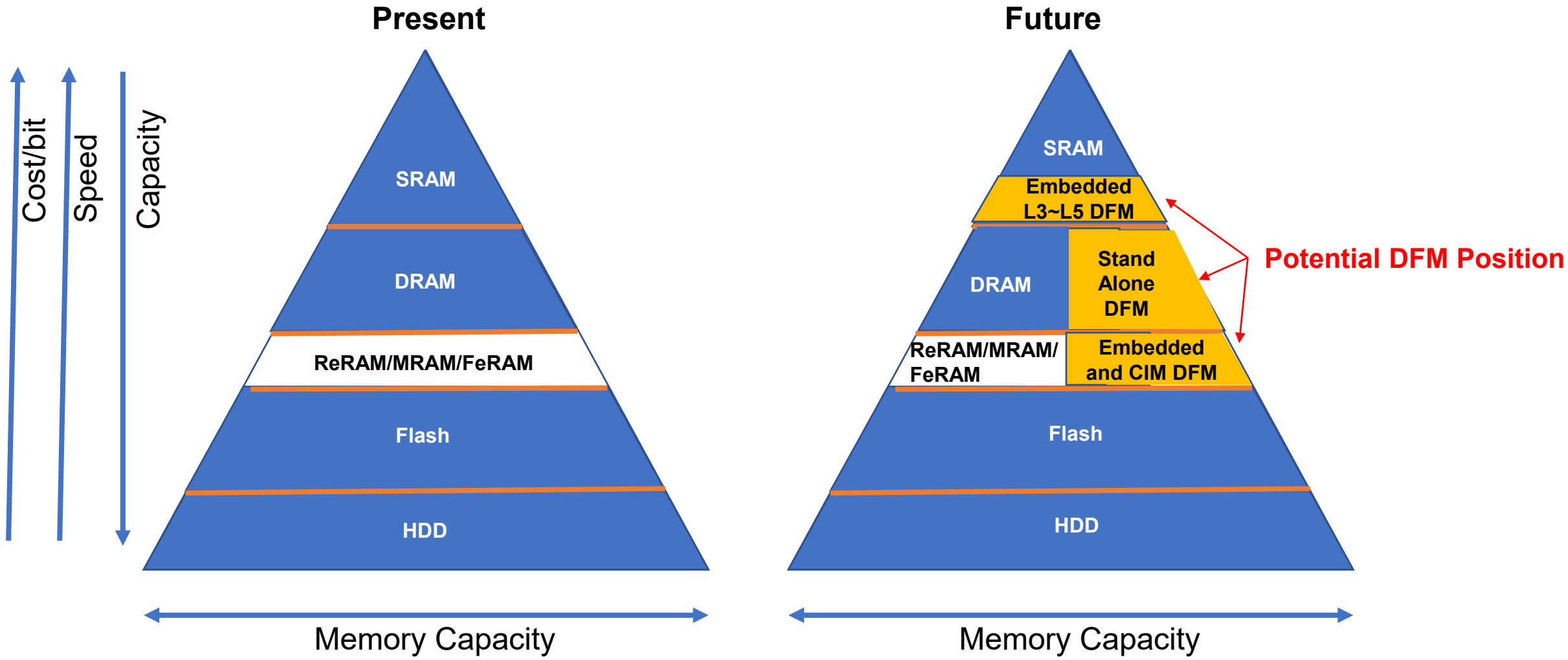
Difficulties in realizing MLC DRAM

1. It is difficult to fulfill a capacitor with four different states.

2. *Bisection Method* cannot be applied for sensing a DRAM cell, because a DRAM cell is *Read Destructive*.



Potential DFM Position



Conclusion

1. The 2bit/cell 3G DFM has been proposed by controlling the number of holes in the FB.

2. Unlike emerging memories, such as ReRAM and MRAM, neither variable resistors nor special materials are needed. It should be noted that DFM can be fabricated with the conventional Si process.

3. A low cost stackable DFM is a promising device positioned next to DRAM and NAND in the memory hierarchy.