OMEM-202-1: Life Beyond Flash 8/9/2023 9:45 AM

Flash Memory Summit

Stacked Dynamic Flash Memory (DFM) for a High Density Memory

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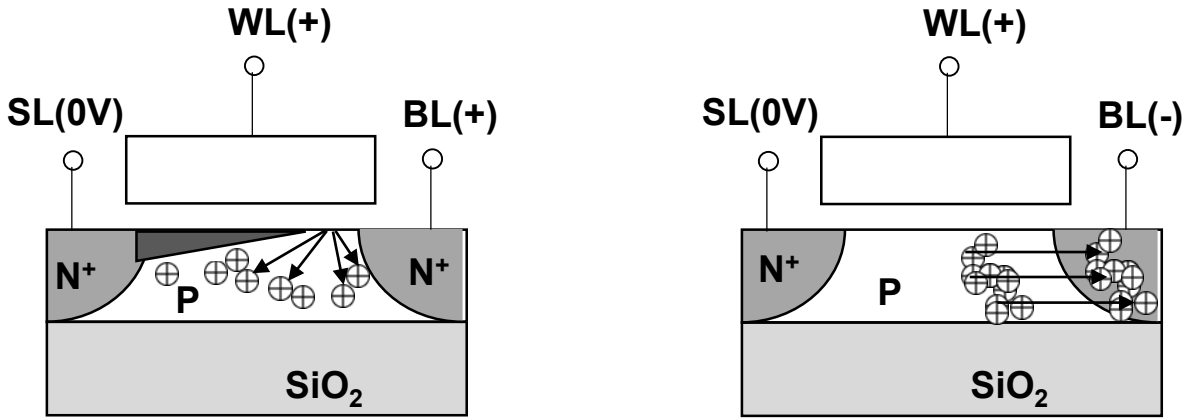
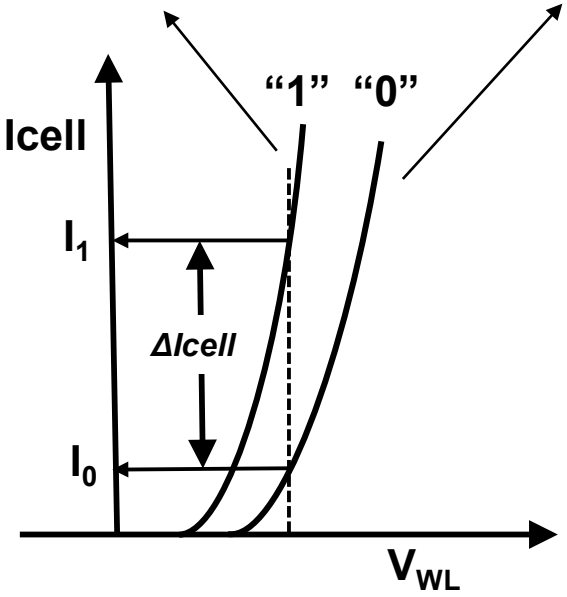
Stacked Dynamic Flash Memory

1. 3G_DFM Introduction
2. Stacked DFM Structure
3. Stacked DFM Prospects and Potential
4. Conclusion

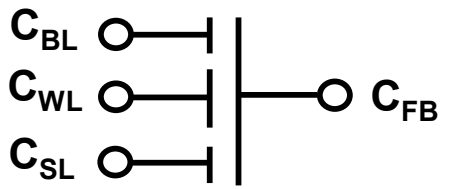
1T-DRAM "1" Program and "0" Erase Mechanism



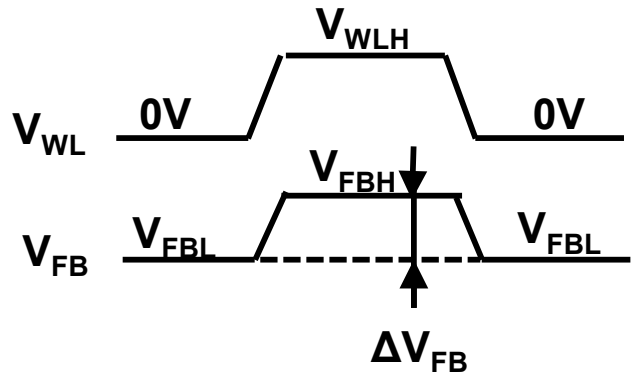


Concerning

1. Large WL capacitive coupling to FB
2. Small "1" and "0" margin
   1. Cell Vth is defined by WL
   2. Negative WL is required for maintaining "1"



$$C_{FB} = C_{WL} + C_{BL} + C_{SL}$$



$$\beta_{WL} = \frac{C_{WL}}{C_{WL} + C_{BL} + C_{SL}} \Rightarrow \text{Large } \beta_{WL}$$

$$\Delta V_{FB} = V_{FBH} - V_{FBL}$$

$$= \underbrace{\beta_{WL} \times V_{WLH}}_{\text{Large}}$$

1. K. Sakui, "Semiconductor Storage Device," *Japanese Patent Application* Number: 01-311386, Publication Number: 03-171768, Filed on Nov. 30, 1989. https://www.j-platpat.inpit.go.jp/c1800/PU/JP-H03-171768/FB67F895FBFE2F6E87B65C8C6F657C4AF31A01A65ED0C2F6EC8D0EF1473CECCA/11/en

“1” Program and “0” Erase Mechanism

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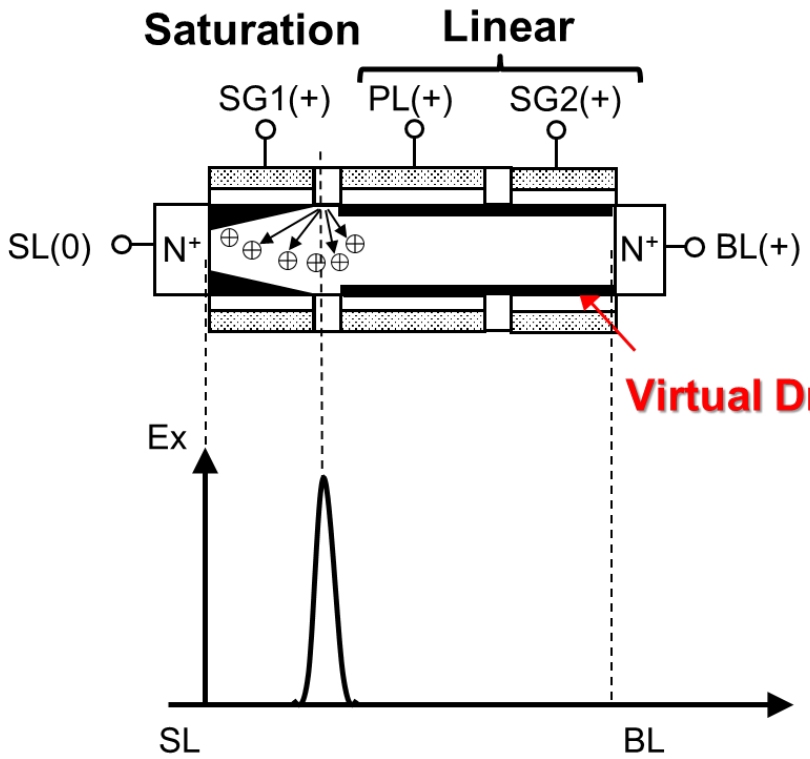
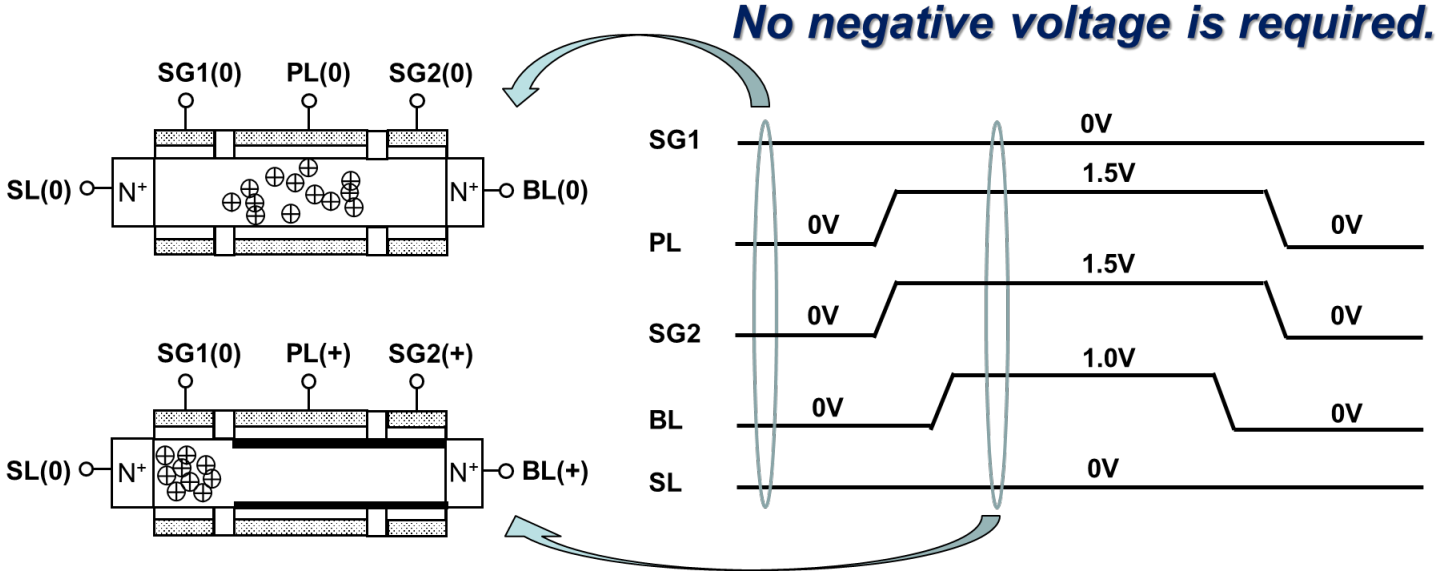
“1” Program

“0” Erase

~Source-side Impact Ionization~



No negative voltage is required.



K. Sakui, Y. Li, M. Kakumu, K. Kanazawa, I. Kunishima, Y. Iwata, and N. Harada, “Design Impact on Three Gate Dynamic Flash Memory (3G_DFM) for Long Hole Retention Time and Robust Disturbance Shield,” in *Memories - Materials, Devices, Circuits and Systems, Elsevier*, 4, 100054, pp.1-5, May 2023.

Wide “1”-“0” Margin

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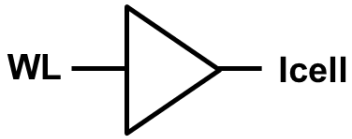
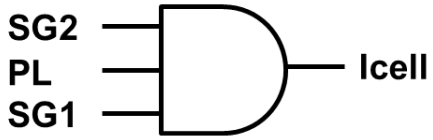
Logical Expression



WL	Icell
1	1
0	0

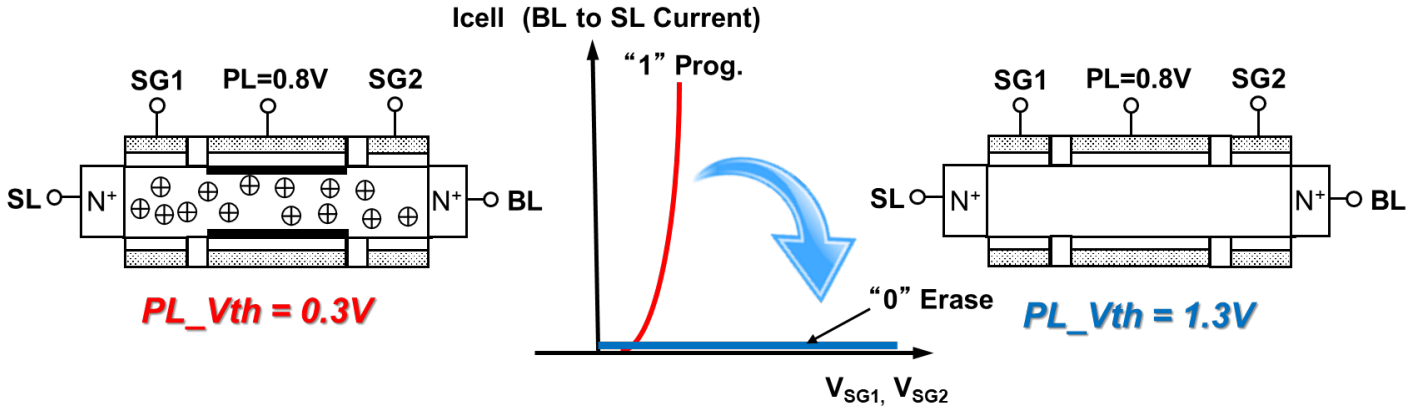
(a) 1T-DRAM



SG1	PL	SG2	Icell
1	1	1	1
1	1	0	0
1	0	1	0
1	0	0	0
0	1	1	0
0	1	0	0
0	0	1	0
0	0	0	0

(b) 3G_DFM

PL plays a storage, while SG1/SG2 plays a switch !



A fixed voltage of 0.8V is applied to PL on reading.

K. Sakui, Y. Li, M. Kakumu, K. Kanazawa, I. Kunishima, Y. Iwata, and N. Harada, “Design Impact on Three Gate Dynamic Flash Memory (3G_DFM) for Long Hole Retention Time and Robust Disturbance Shield,” in *Memories - Materials, Devices, Circuits and Systems, Elsevier*, 4, 100054, pp.1-5, May 2023.

The FB Stabilization by the Three Gates

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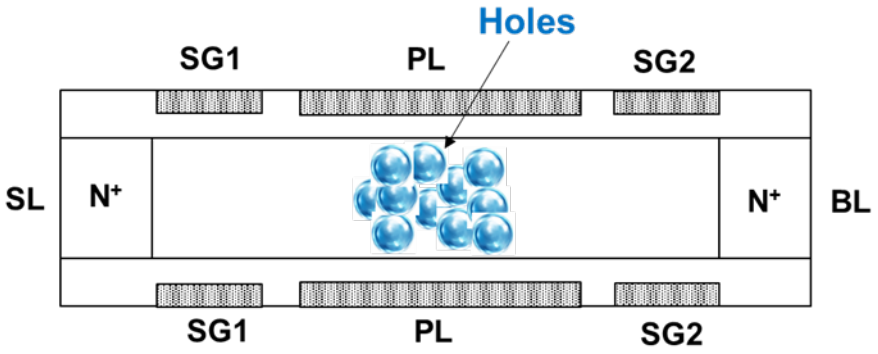
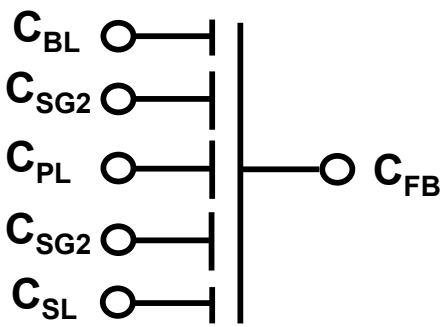
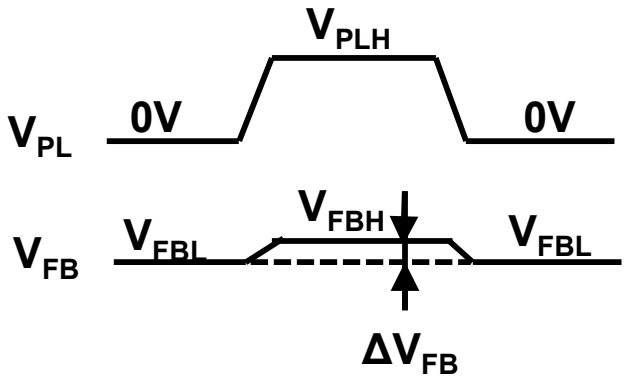
Small gate capacitive coupling to FB !







$$C_{FB} = C_{SG1} + C_{PL} + C_{SG2} + C_{BL} + C_{SL}$$

$$\Delta V_{FB} = V_{FBH} - V_{FBL}$$

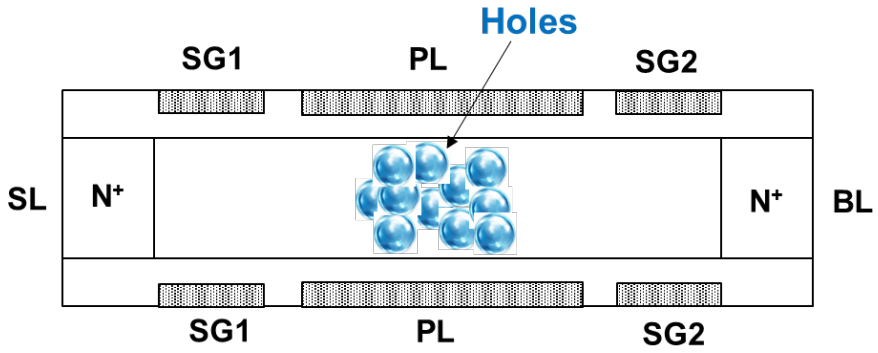
$$= \beta_{PL} \times V_{LPH}$$

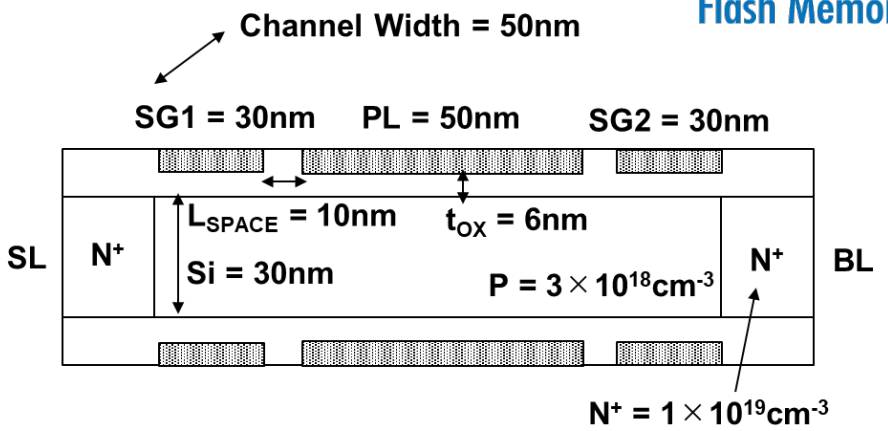
$$\beta_{PL} = \frac{C_{PL}}{C_{SG1} + C_{PL} + C_{SG2} + C_{BL} + C_{SL}} \Rightarrow \text{Small } \beta_{PL}$$

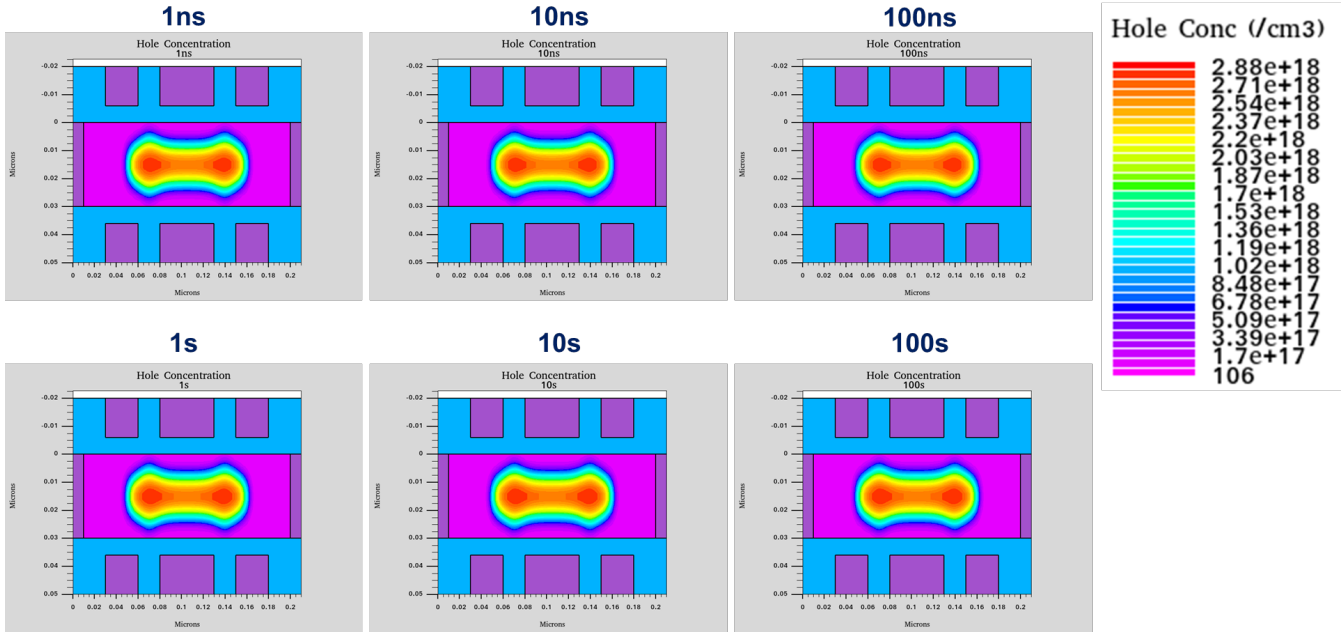
$$= \frac{\text{Small}}{}$$

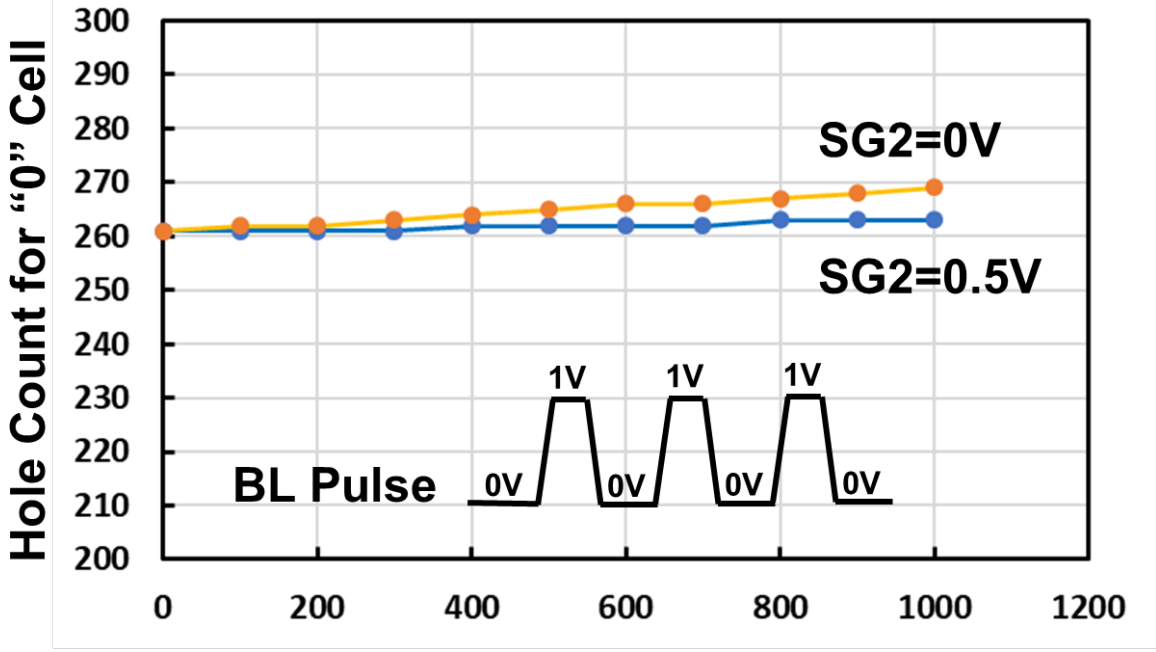
K. Sakui, Y. Li, M. Kakumu, K. Kanazawa, I. Kunishima, Y. Iwata, and N. Harada, "Design Impact on Three Gate Dynamic Flash Memory (3G_DFM) for Long Hole Retention Time and Robust Disturbance Shield," in *Memories - Materials, Devices, Circuits and Systems, Elsevier*, 4, 100054, pp.1-5, May 2023.

3G_DFM Robustness Against Disturbance









Hole Concentration After "1" Write (PL=0V, 85℃)

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3D DRAM Papers

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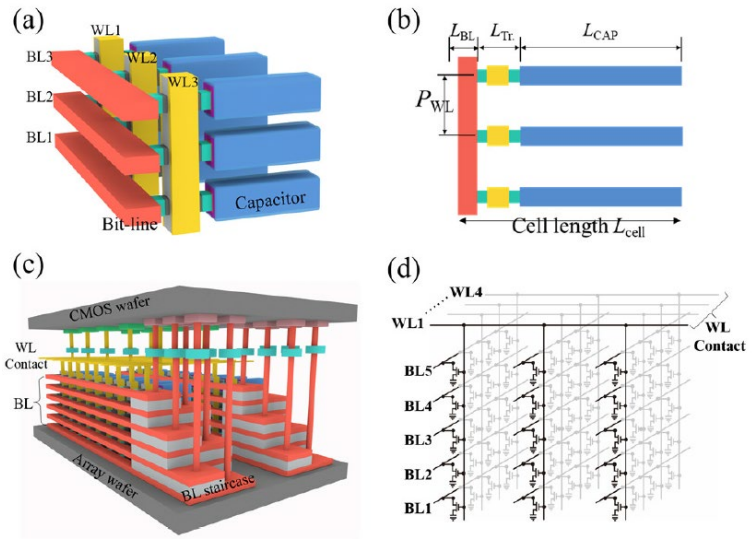
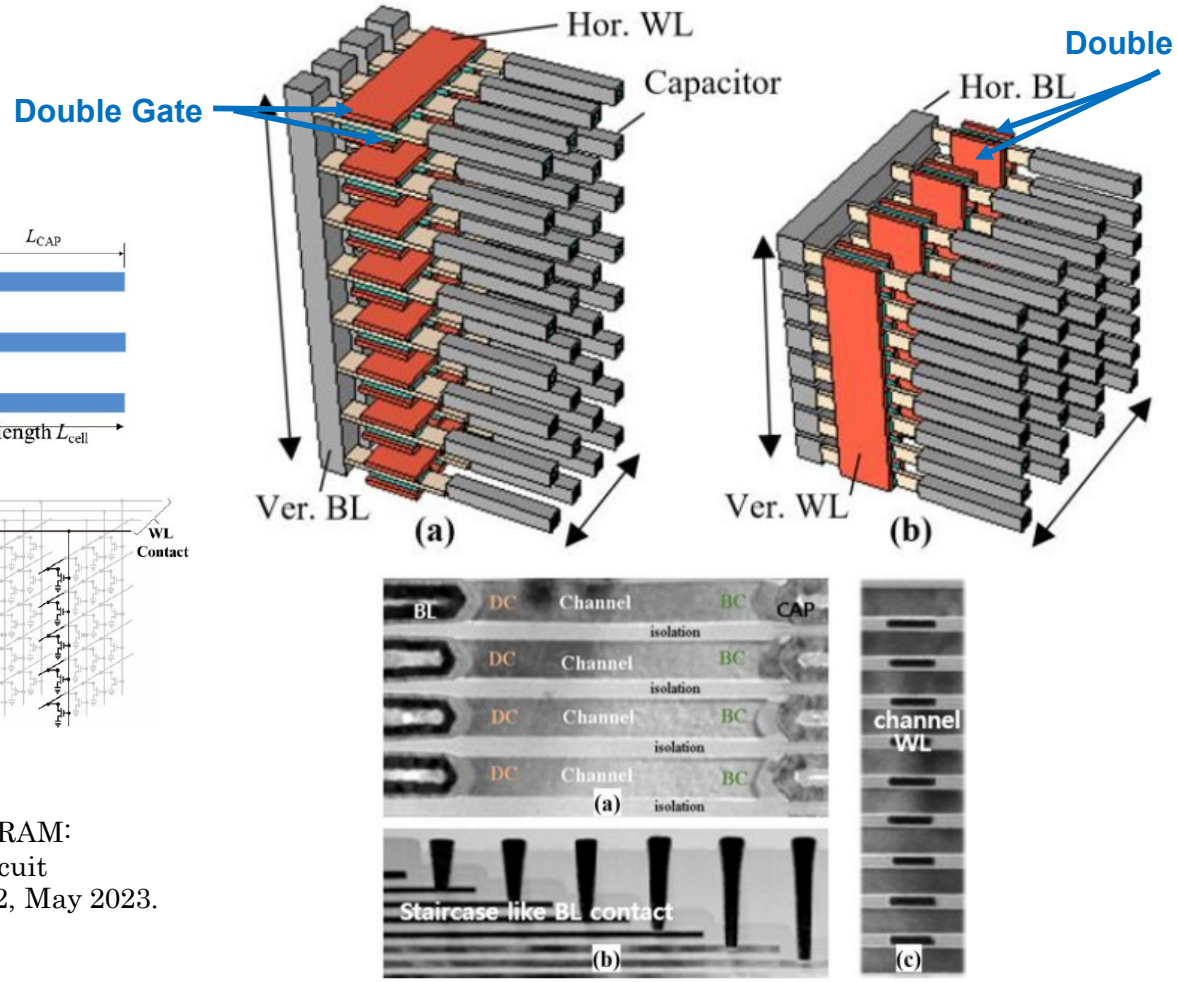
CXMT: Stacked 1T1C
IMW 2023



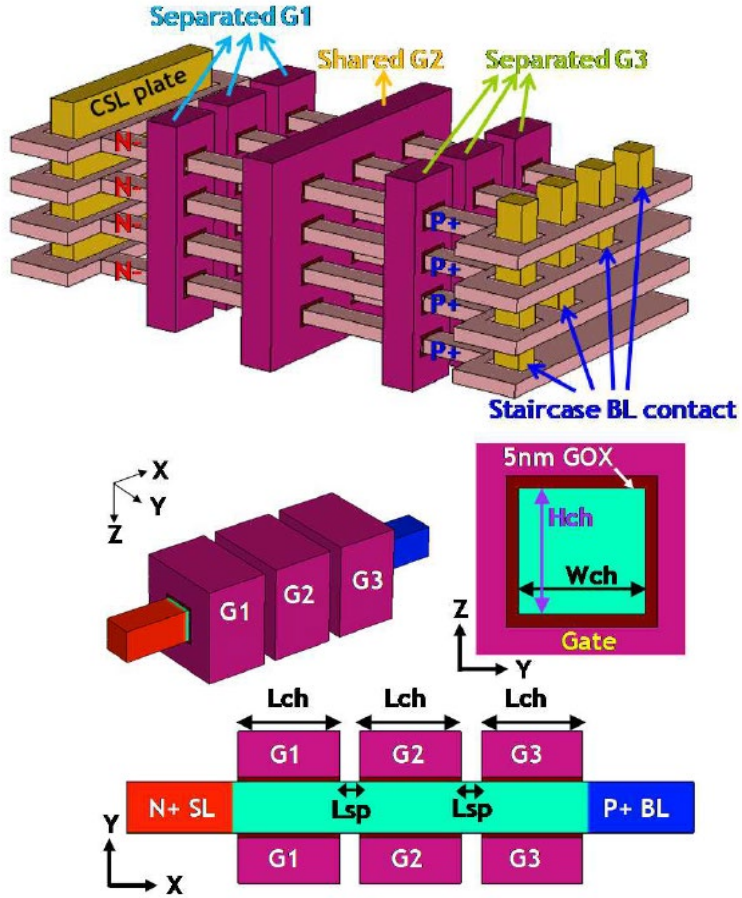
M. Huang et al., "A 3D Stackable 1T1C DRAM: Architecture, Process Integration and Circuit Simulation," in *Proc. IEEE IMW*, pp.29-32, May 2023.

Samsung: Stacked 1T1C
VLSI 2023



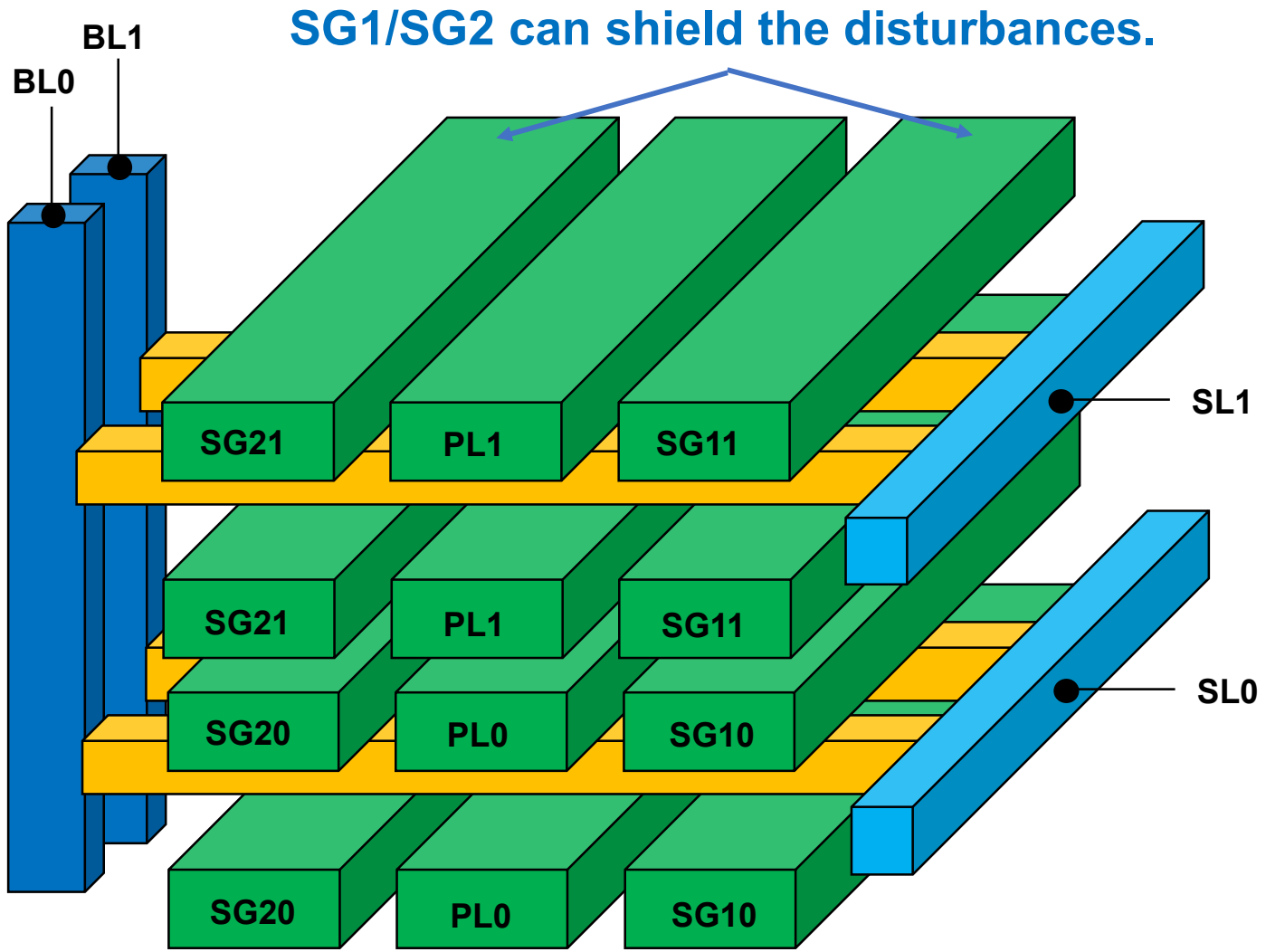
J.W. Han et al., "Ongoing Evolution of DRAM Scaling via Third Dimension - Vertically Stacked DRAM -," in *2023 Symposium on VLSI Technology and Circuits Digest of Technical Papers*, TFS1-1, pp.1-2, Jun. 2023.

Macronix: Stacked Thyristor
IEDM 2022, IMW 2023

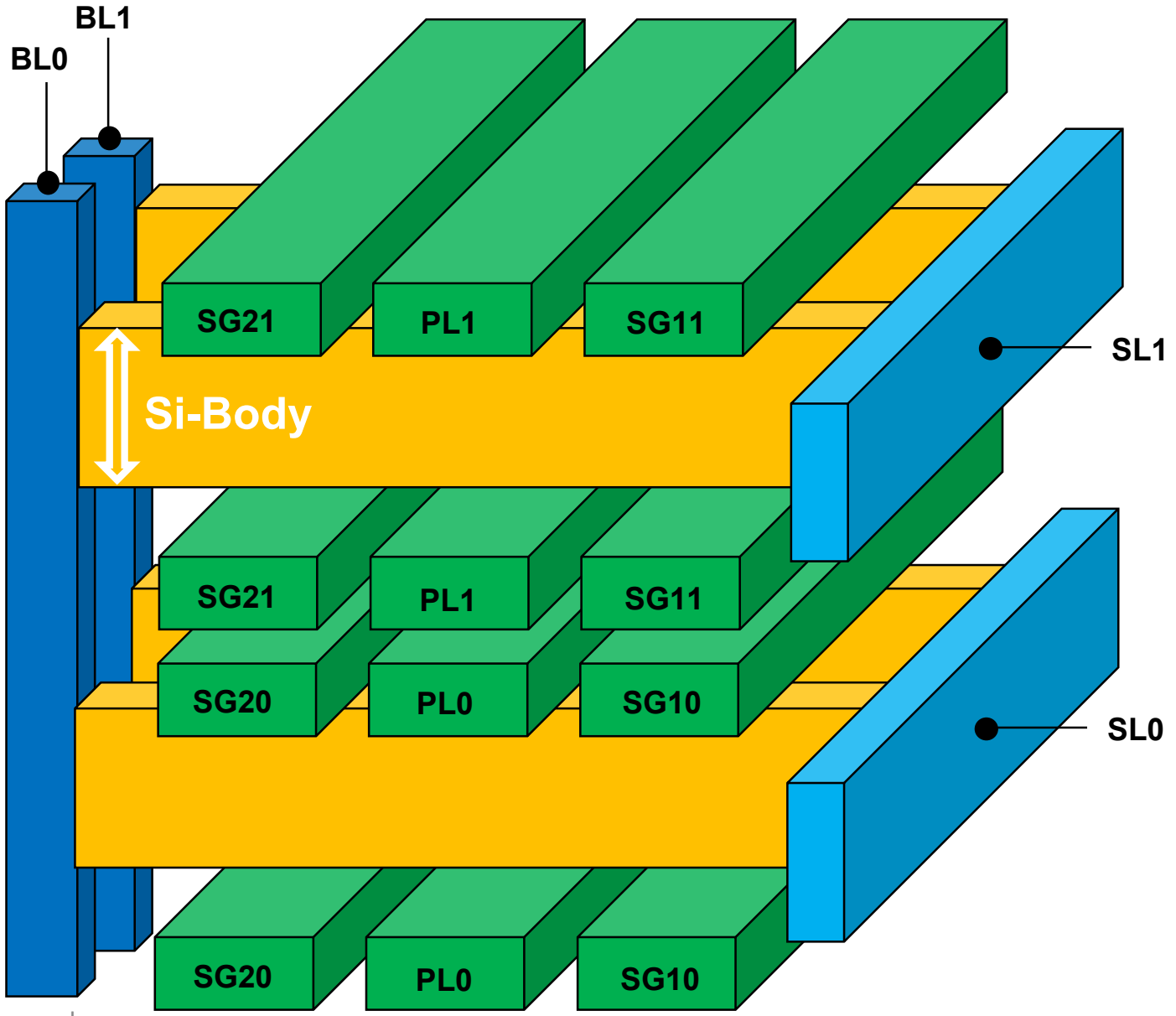


W. C. Chen et al., "A Simulation Study of Scaling Capability toward 10nm for the 3D Stackable Gate-Controlled Thyristor (GCT) DRAM Device," in *Proc. IEEE IMW*, pp.25-28, May 2023.

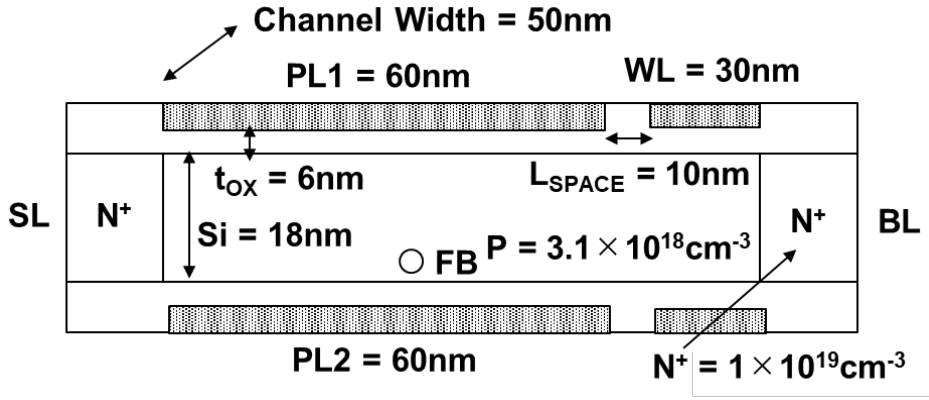
Double Stacked DFM (Horizontal Gates)

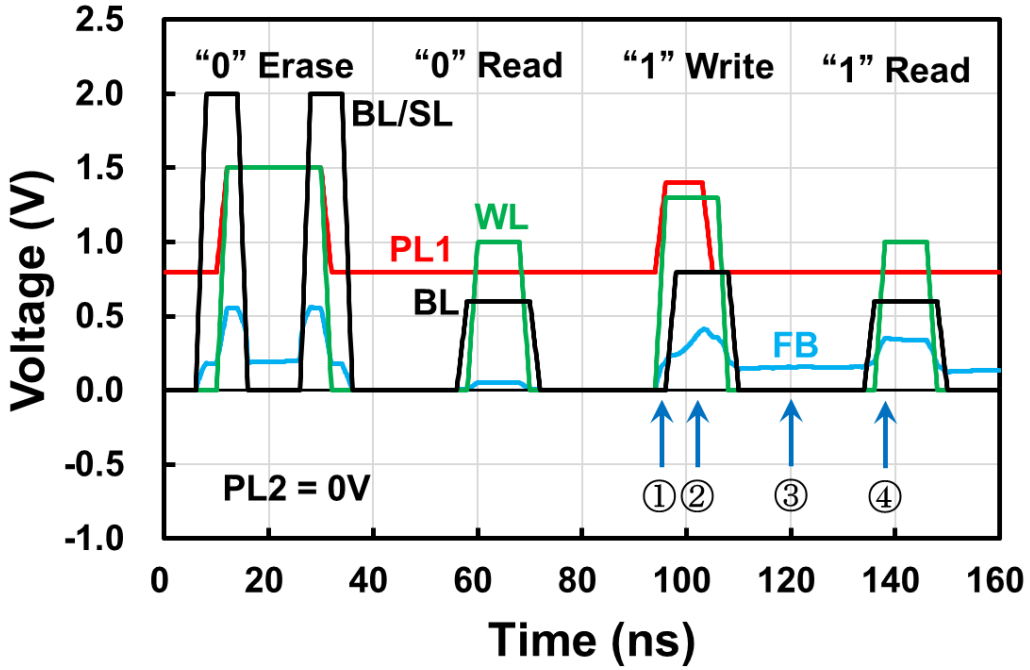


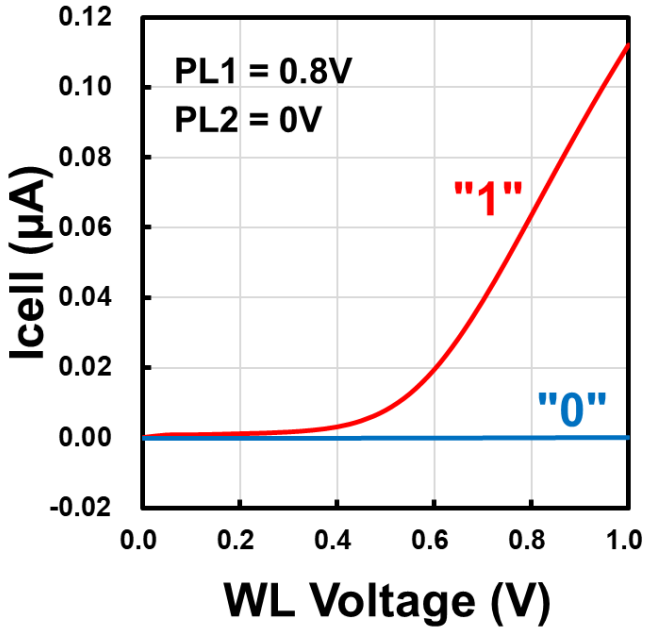
Si-Body Thickness Control without Cell Size Increase



2G_DFM (Double Gate)

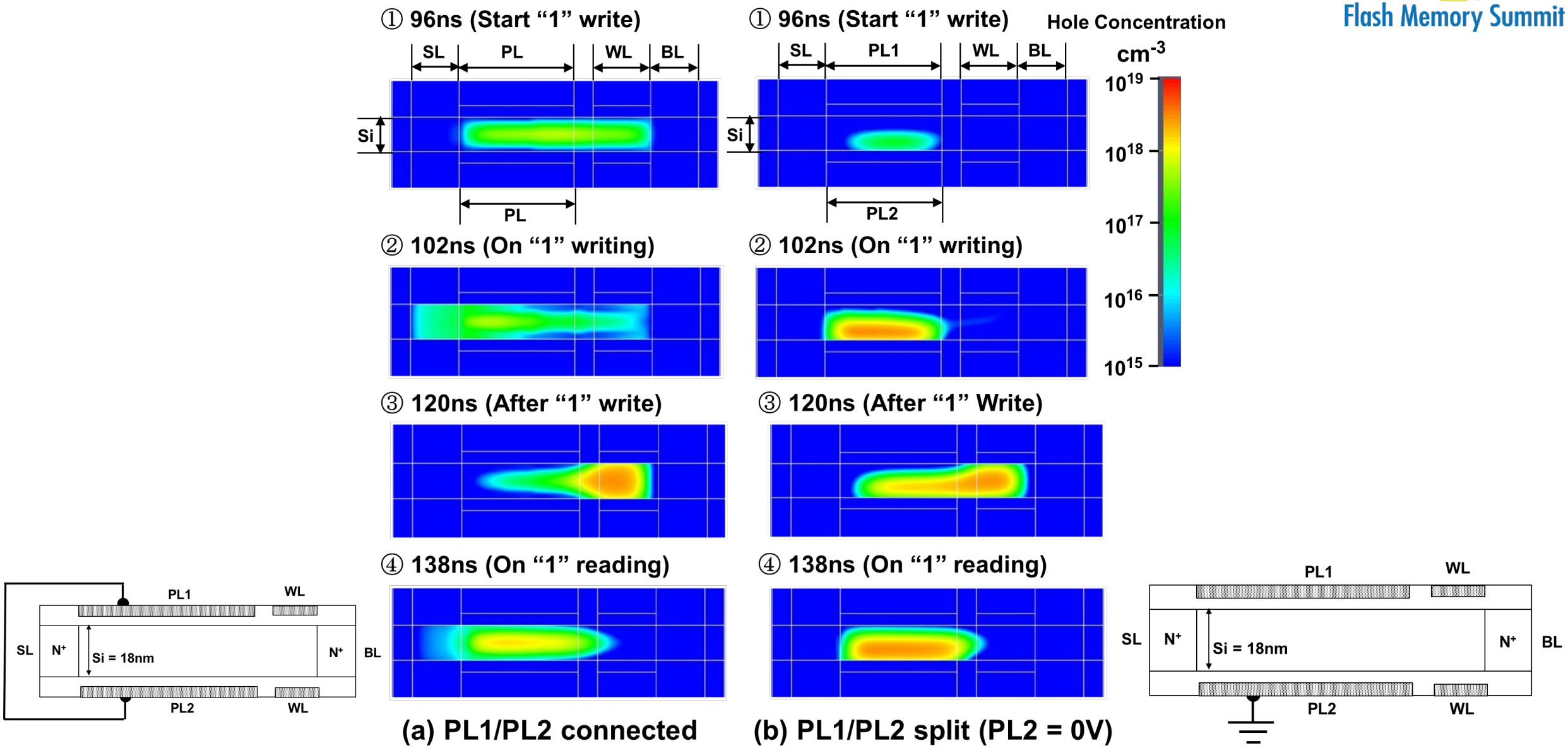




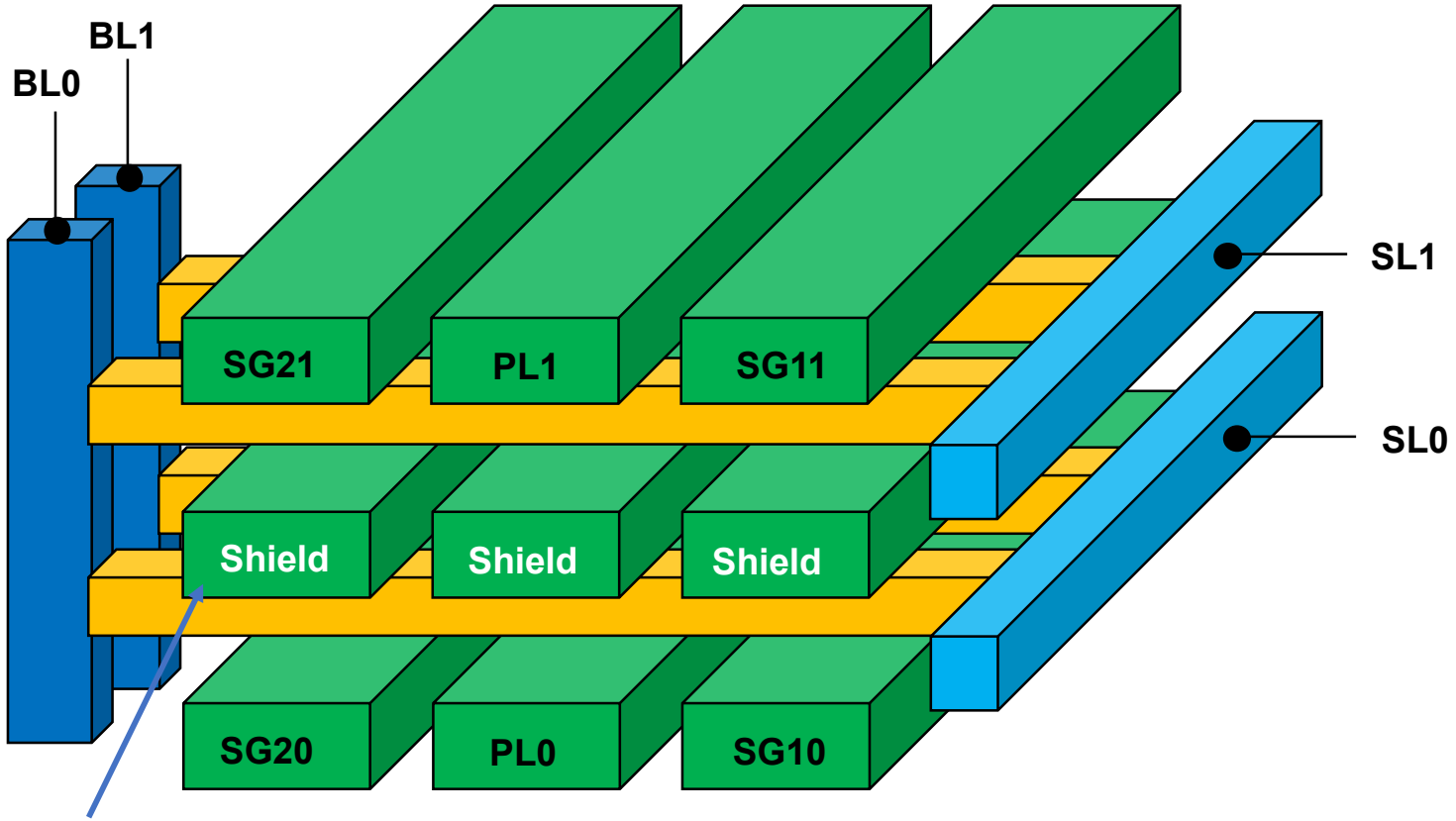


K. Sakui and N. Harada, "Read Non-Destructive Dynamic Flash Memory (DFM) with Dual and Double Gates," in *SSDM*, F-4-02, pp.405-406, Sep. 2022.

Hole concentration: (a) PL1 = PL2, (b) PL2 = 0V

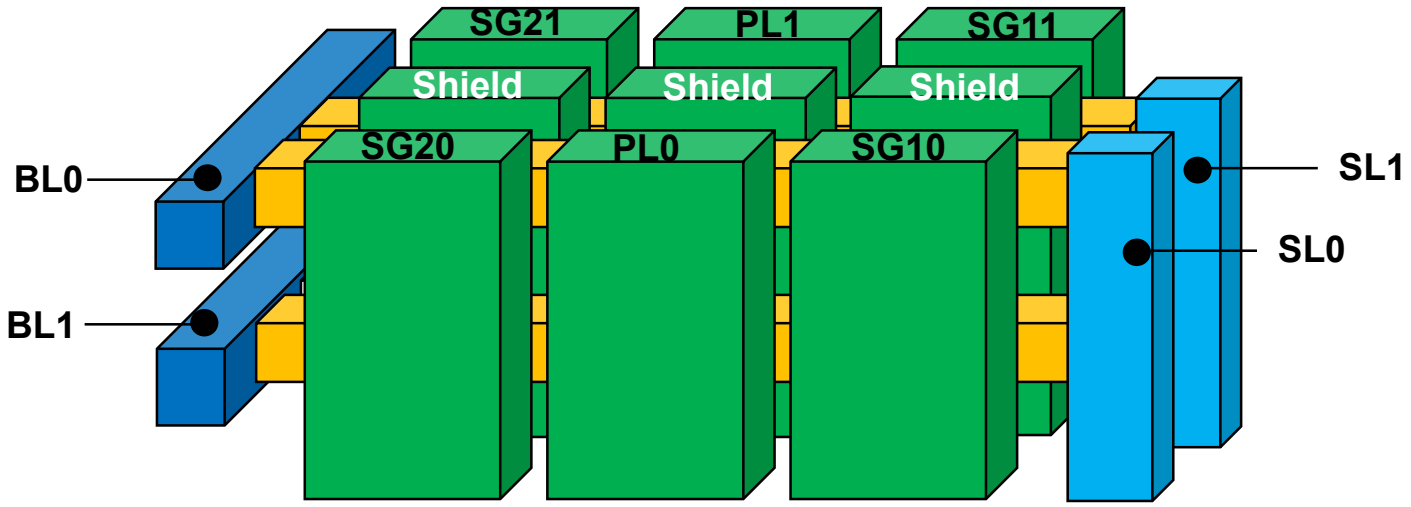


Two Stack DFM (Horizontal Gate)



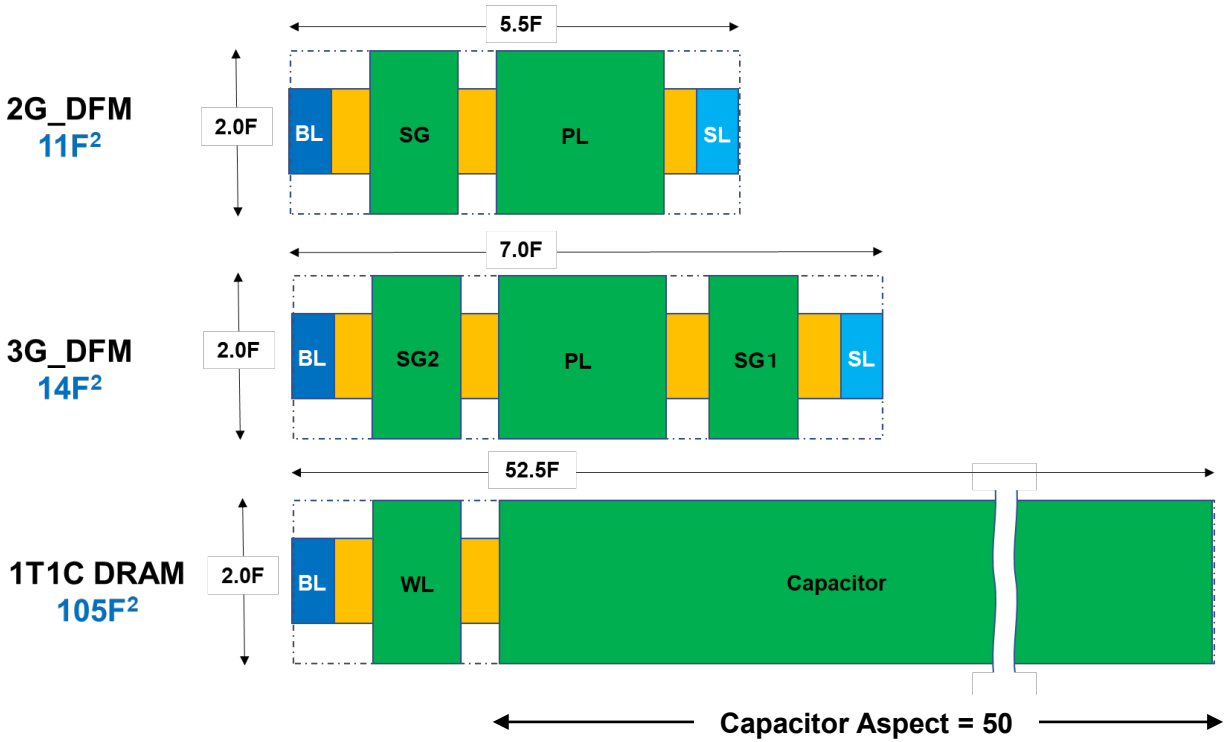
One of double gates is grounded.

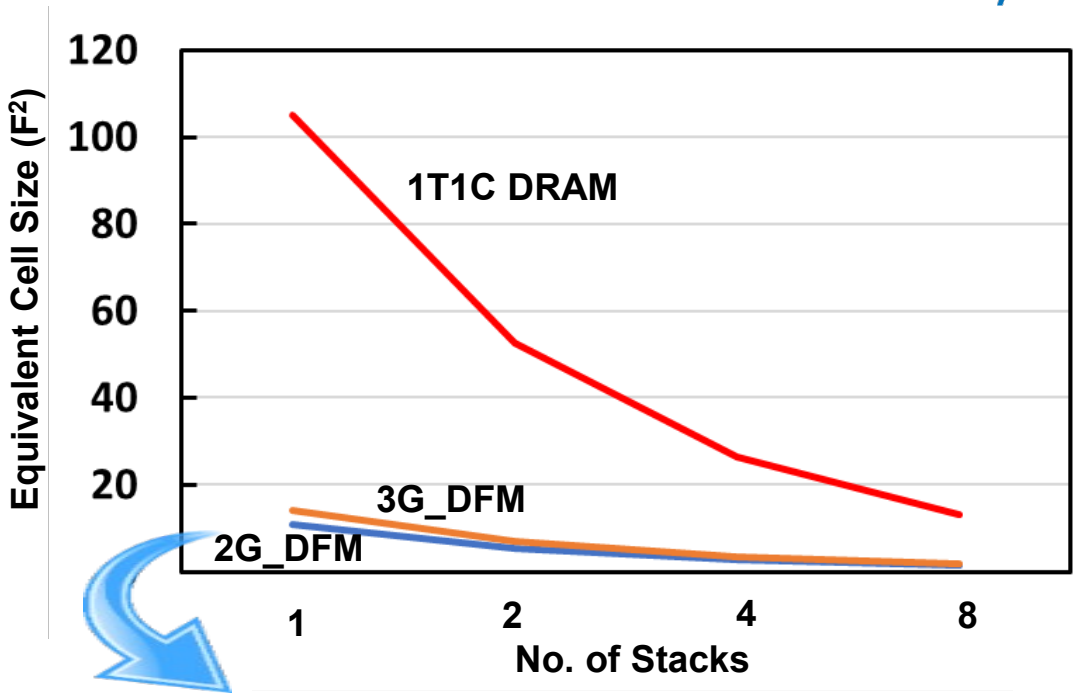
Two Stack DFM (Vertical Gate)

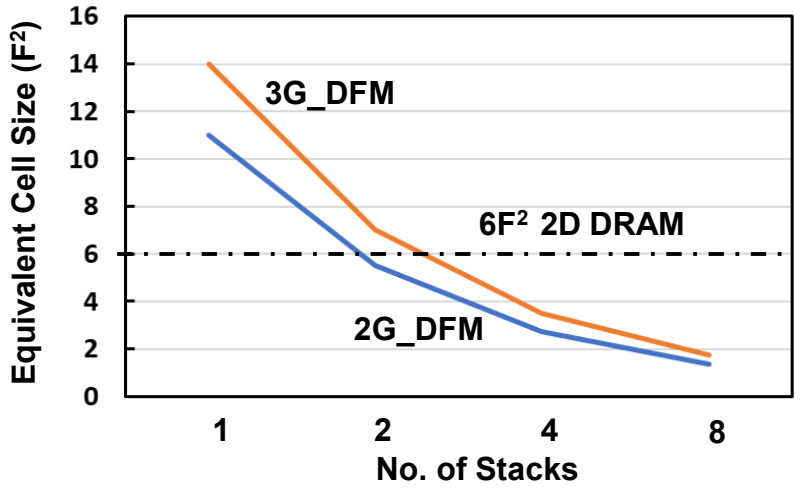


Stacked Dynamic Flash Memory

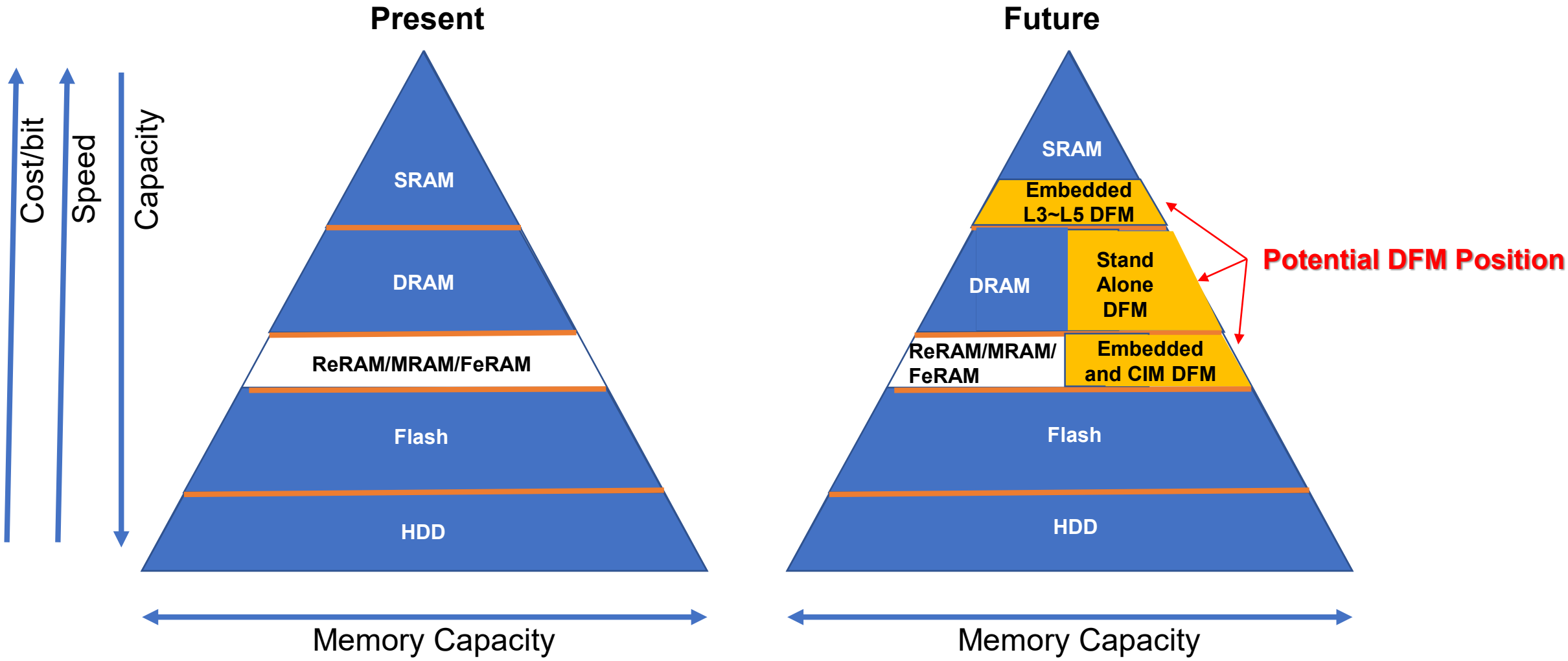
Equivalent Cell Size







Potential DFM Position



Stacked Dynamic Flash Memory

1. 3G_DFM Introduction
2. Stacked DFM Structure
3. Stacked DFM Prospects and Potential
4. **Conclusion**

Conclusion

1. The stacked 3G_DFM has a substantial potential to realize a much smaller equivalent cell than $6F^2$ with 3~4 tiers.

2. Unlike emerging memories, such as ReRAM and MRAM, neither variable resistors nor special materials are needed. It should be noted that DFM can be fabricated with the conventional Si process.

3. A low cost stackable DFM is a promising device positioned next to DRAM and NAND in the memory hierarchy.