Short Course 2: The Future of Memory Technologies for High-Performance Memory and Computing
9:00 - 18:00 on December 10, 2023

High-Density and High-Performance Technologies for Future Memory

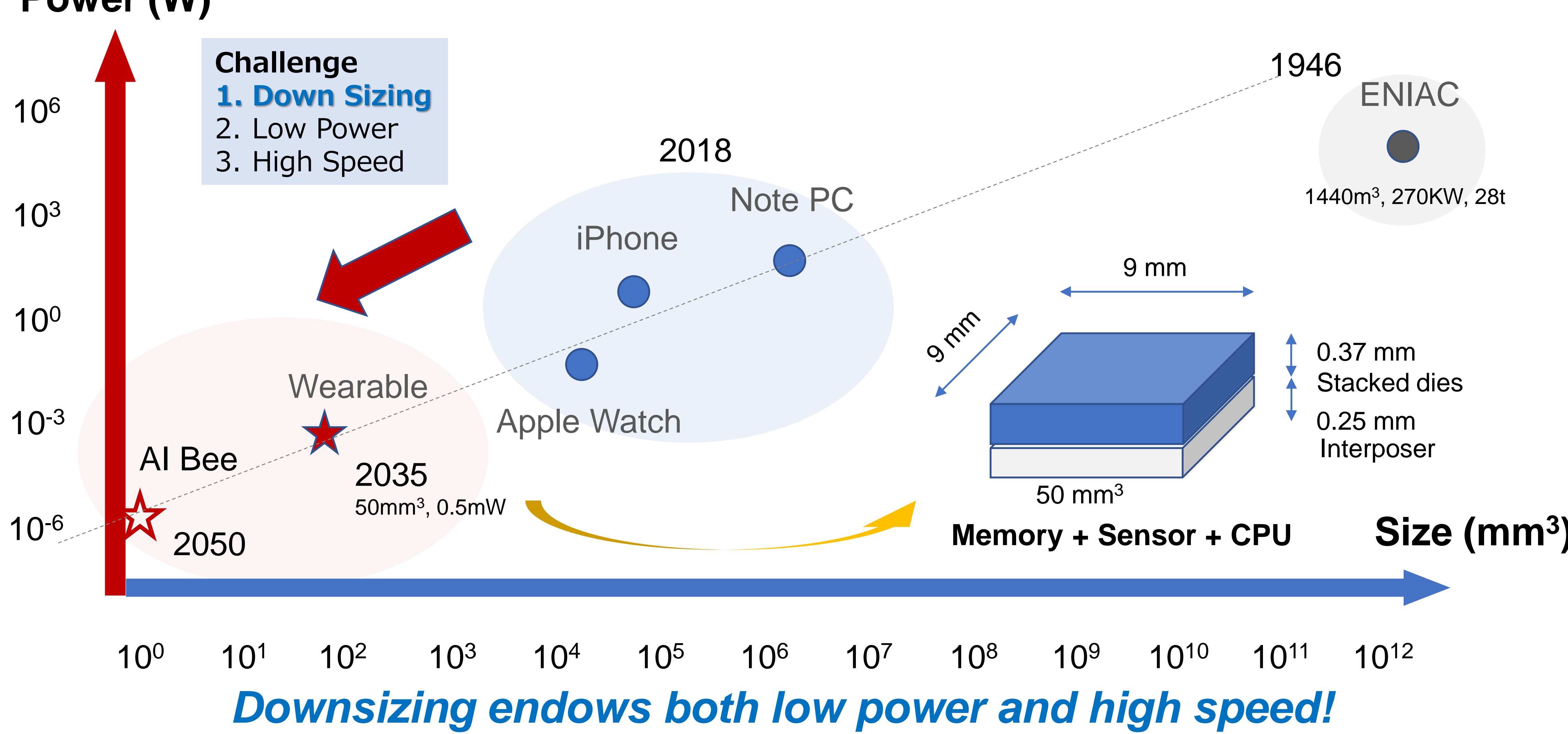
Koji Sakui

Unisantis Electronics Singapore,

60 Paya Lebar Road, #10-49, Paya Lebar Square, Singapore 409051 sakui@unisantis.com

Let’s imagine,,,

The World in 2050 AD



Downsizing endows both low power and high speed!

1. K. Sakui and T. Ohba, "Three-dimensional Integration (3DI) with Bumpless Interconnects for Tera-scale Generation," in *the IEEE CICC Dig. Tech. Papers*, 22-6, April 2019.
2. K. Sakui and T. Ohba, "High Speed, Low Power, and Ultra-small Operating Platform with Three-dimensional Integration (3DI) by Bumpless interconnects," in *the IEEE IMW Dig. Tech. Papers*, pp.60-63, May 2019.
3. K. Sakui and T. Ohba, "High Bandwidth Memory (HBM) and High Bandwidth NAND (HBN) with the Bumpless TSV Technology," in *the IEEE 2019 International 3D Systems Integration Conference Dig. Tech. Papers*, Paper Id: 3DIC2019.4005, Oct 2019.

Semiconductor Memories

DRAM: R. H. Dennard, "Field-Effect Transistor Memory," *U.S.P. 3,387,286*, Filed on Jul. 14, 1967.

Flash: F. Masuoka, "Semiconductor Memory Device," *U.S.P. 4,437,174*, Filed on Jan. 19, 1981 (Japan)..

An enormous number of ideas have been emerged after DRAM and Flash.

Questions are

1. What is the key specification of emerging memories in comparison with DRAM and NAND?
    1. Cost
    2. Speed
    3. Power
    4. Any others
2. What is the merit of using different materials from the conventional Si process?

Agenda

1. DFM: Dynamic Flash Memory
2. KFBM: Key shape Floating Body Memory
3. SGT: Surrounding Gate Transistor
4. BBCube: Bumpless Build Cube

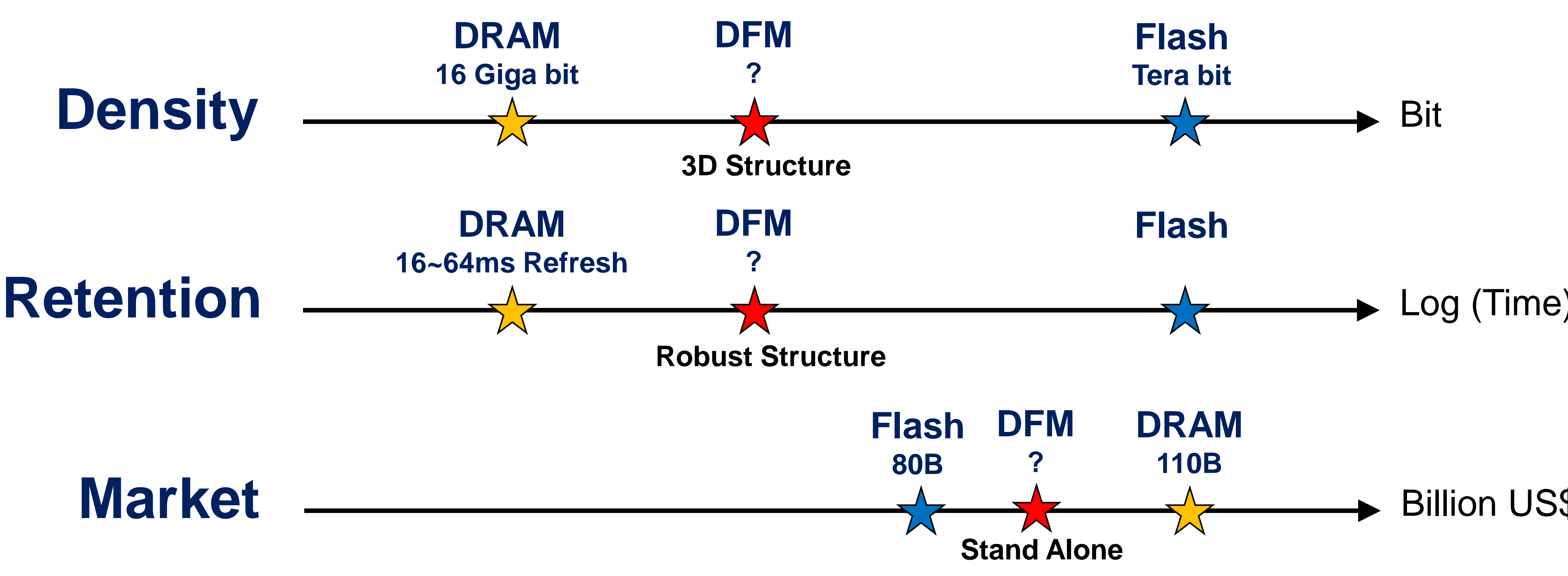
Agenda

1. DFM: Dynamic Flash Memory
2. KFBM: Key shape Floating Body Memory
3. SGT: Surrounding Gate Transistor
4. BBCube: Bumpless Build Cube

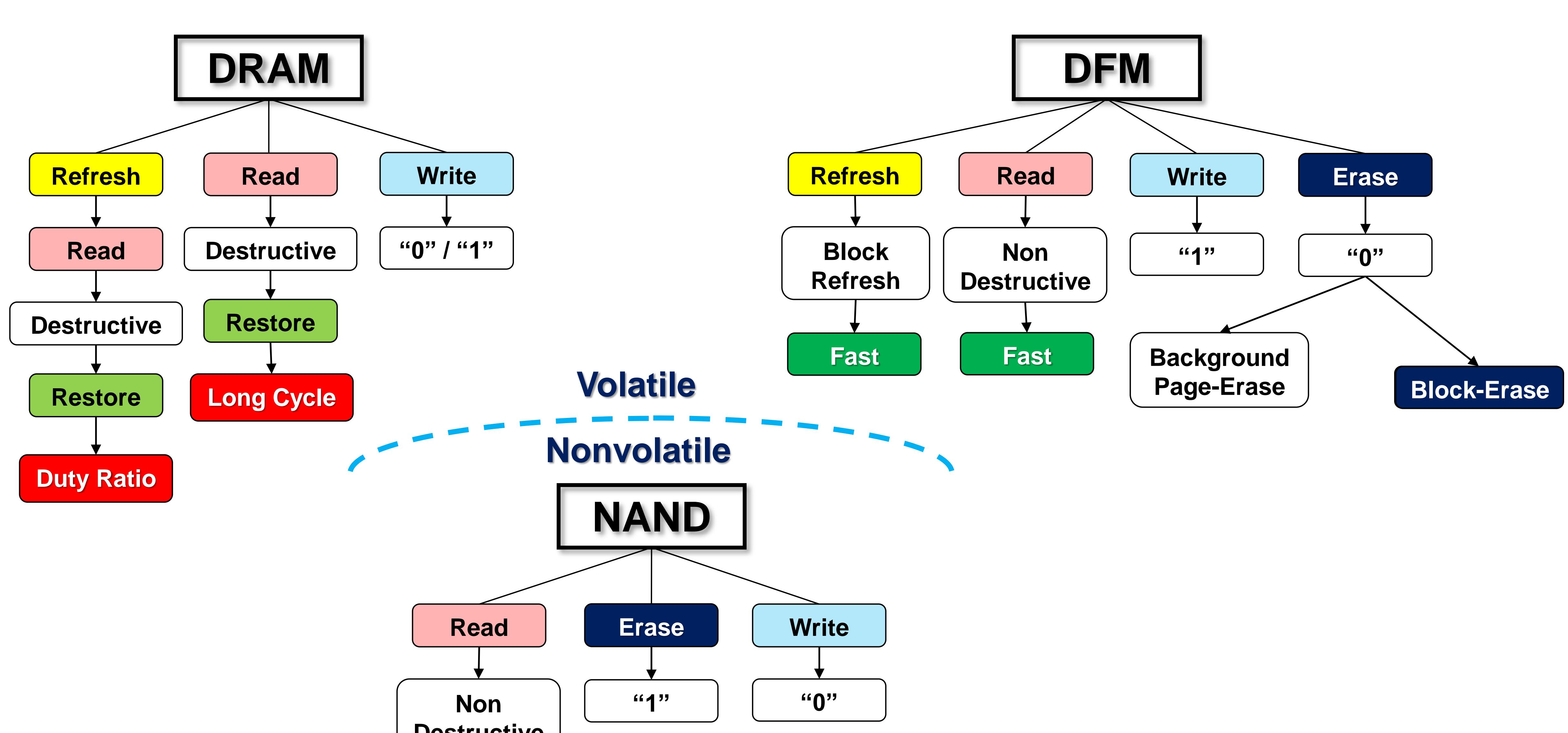
DFM's Dynamic Life Start ⇒ Agenda Horizon

DFM was just born three years ago.

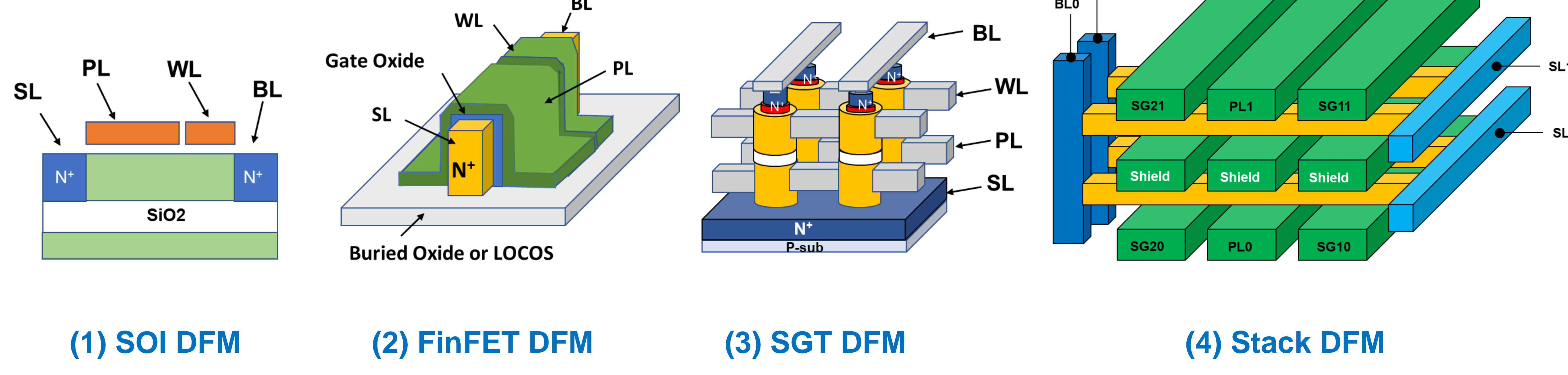
K. Sakui and N. Harada, "Memory Device with Semiconductor Device," *Japanese Patent Number*: 7057032, Filed on Dec. 25, 2020.



DFM Concept

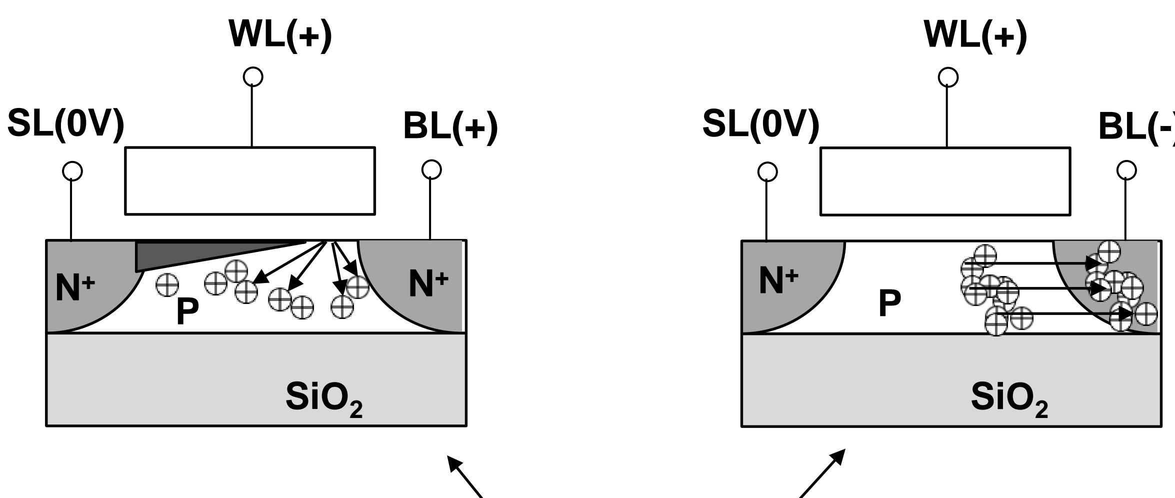


DFM Structure



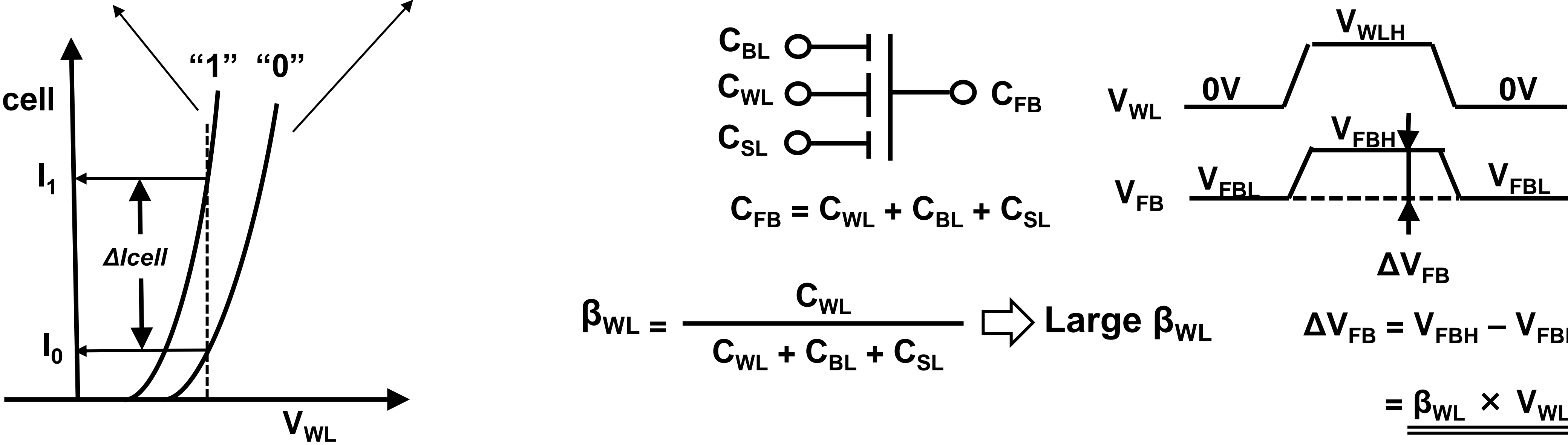
(1) SOI DFM (2) FinFET DFM (3) SGT DFM (4) Stack DFM

1T-DRAM (Z-RAM)



Concerning

1. Large WL capacitive coupling to FB
2. Small "1" and "0" margin
   1. Cell Vth is defined by WL
   2. Negative WL is required for maintaining "1"



K. Sakui, "Semiconductor Storage Device," *Japanese Patent Application* Number: 01-311386, Publication Number: 03-171768, Filed on Nov. 30, 1989.
https://www.j-platpat.inpit.go.jp/c1800/PU/JP-H03-171768/FB67F895FBFE2F6E87B65C8C6F657C4AF31A01A65ED0C2F6EC8D0EF1473CECCA/11/en

A New Static Memory Cell Based on the Reverse Base Current Effect of Bipolar Transistor

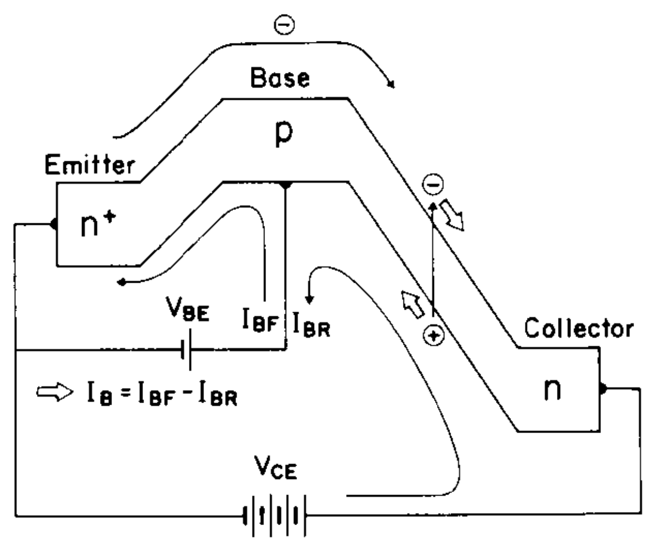


Fig. 1. RBC effect mechanism.

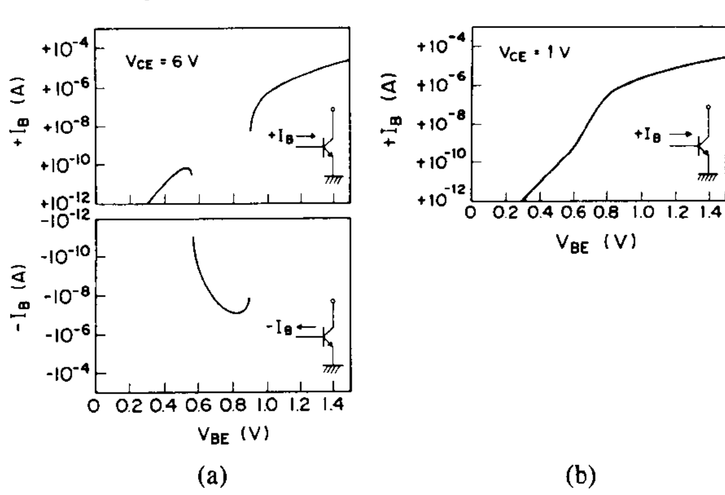


Fig. 2. Measured base current versus V_{BE} at (a) V_{CE} = 6 V and (b) V_{CE} = 1 V.

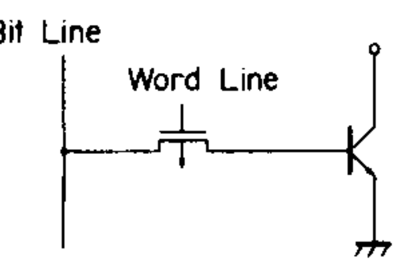


Fig. 6. Equivalent RBC cell circuit

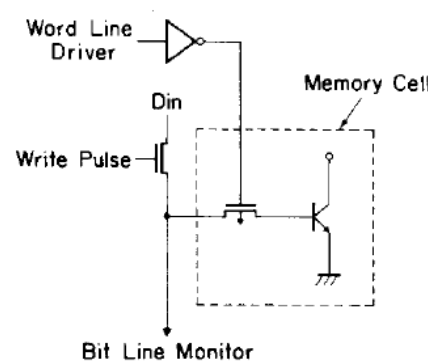


Fig. 9. Memory cell and monitor circuit.

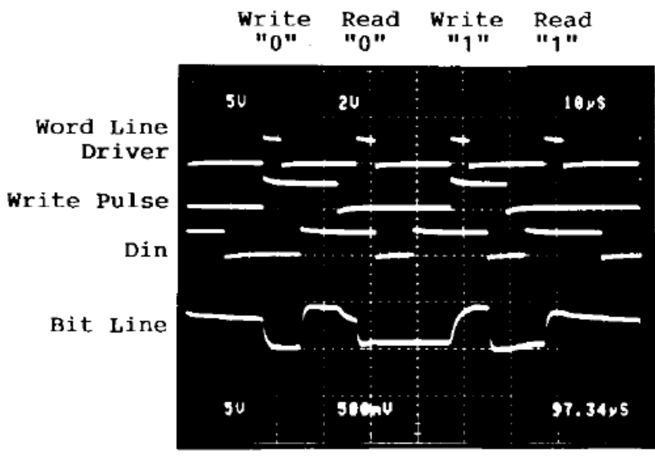


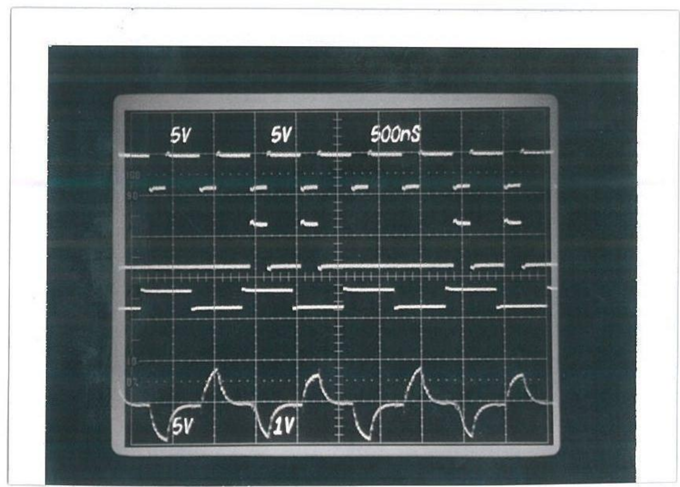
Fig. 10. Operation characteristics of RBC cell. The horizontal time scale is 10 μs/div. The vertical voltage scale is 5 V/div for word line driver and write pulse, 2 V/div for din, and 500 mV/div for bit line.

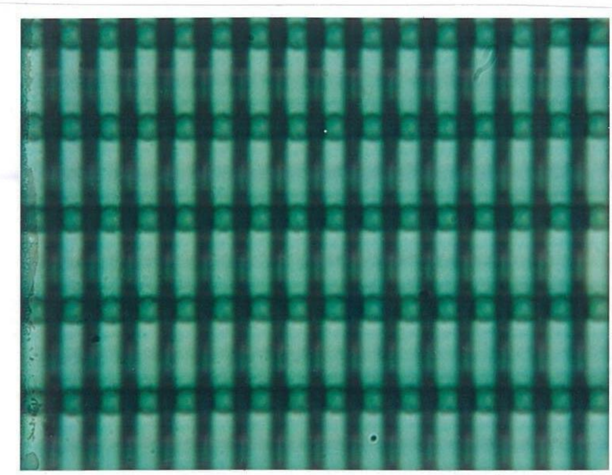
1. K. Sakui, T. Hasegawa, T. Fuse, S. Watanabe, K. Ohuchi, and F. Masuoka, “A New Static Memory Cell Based on Reverse Base Current (RBC) Effect of Bipolar Transistor,” in *1988 IEDM*, pp.44-47, Dec. 1988.
2. K. Sakui, T. Hasegawa, T. Fuse, S. Watanabe, K. Ohuchi, and F. Masuoka, “A New Static Memory Cell Based on Reverse Base Current (RBC) Effect of Bipolar Transistor,” in *IEEE Trans. Electron Devices*, vol. 36, No. 6, pp.1215-1217, Jum. 1989.

A New Static Memory Cell Based on the Reverse Base Current Effect of Bipolar Transistor

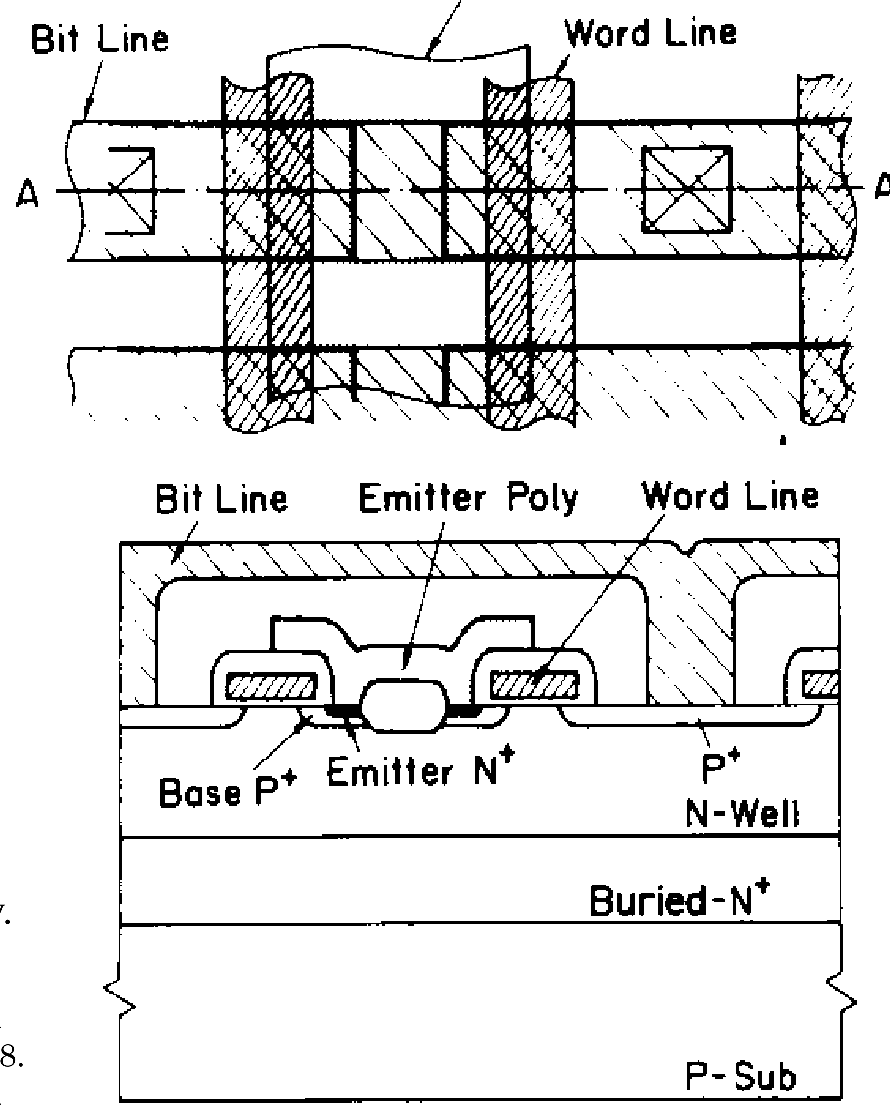
The RBC cell array has been successfully functioned!

(Unpublished Data: Year 1988)





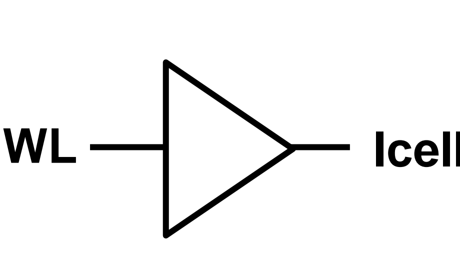
Two memory cells are connected to the same bitline. One of two cells is written “1” and the other is written “0”, and then “1” cell is read and “0” cell is read consecutively.



Top and cross-sectional views for RBC cell.

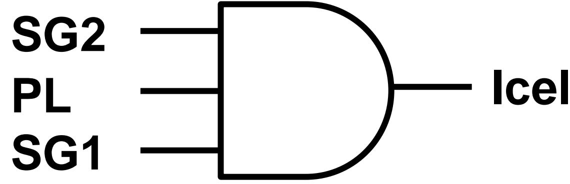
1. K. Sakui, T. Hasegawa, T. Fuse, S. Watanabe, K. Ohuchi, and F. Masuoka, “A New Static Memory Cell Based on Reverse Base Current (RBC) Effect of Bipolar Transistor,” in *1988 IEDM*, pp.44-47, Dec. 1988.
2. K. Sakui, T. Hasegawa, T. Fuse, S. Watanabe, K. Ohuchi, and F. Masuoka, “A New Static Memory Cell Based on Reverse Base Current (RBC) Effect of Bipolar Transistor,” in *IEEE Trans. Electron Devices*, vol. 36, No. 6, pp.1215-1217, Jum. 1989.

Logical Expression



WL	Icell
1	1
0	0

(a) 1T-DRAM



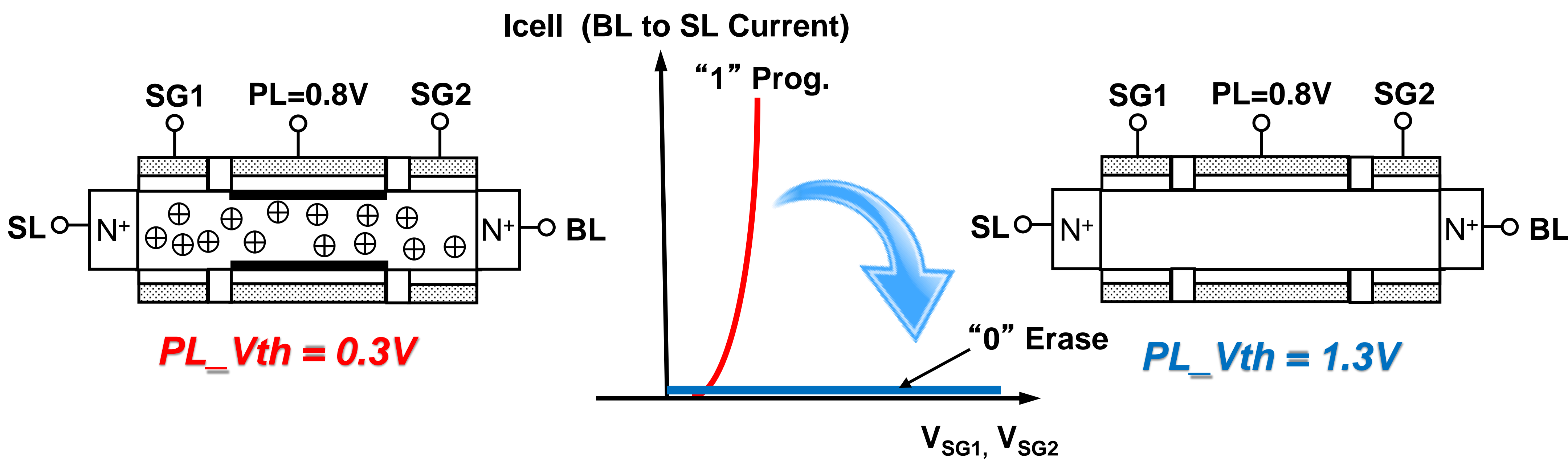
SG1	PL	SG2	Icell
1	1	1	1
1	1	0	0
1	0	1	0
1	0	0	0
0	1	1	0
0	1	0	0
0	0	1	0
0	0	0	0

(b) 3G DFM

K. Sakui, Y. Li, M. Kakumu, K. Kanazawa, I. Kunishima, Y. Iwata, and N. Harada, "Design Impact on Three Gate Dynamic Flash Memory (3G_DFM) for Long Hole Retention Time and Robust Disturbance Shield," in *Memories - Materials, Devices, Circuits and Systems, Elsevier*, 4, 100054, pp.1-5, May 2023.

Wide "1"-"0" Margin

PL plays a storage, while SG1/SG2 plays a switch !

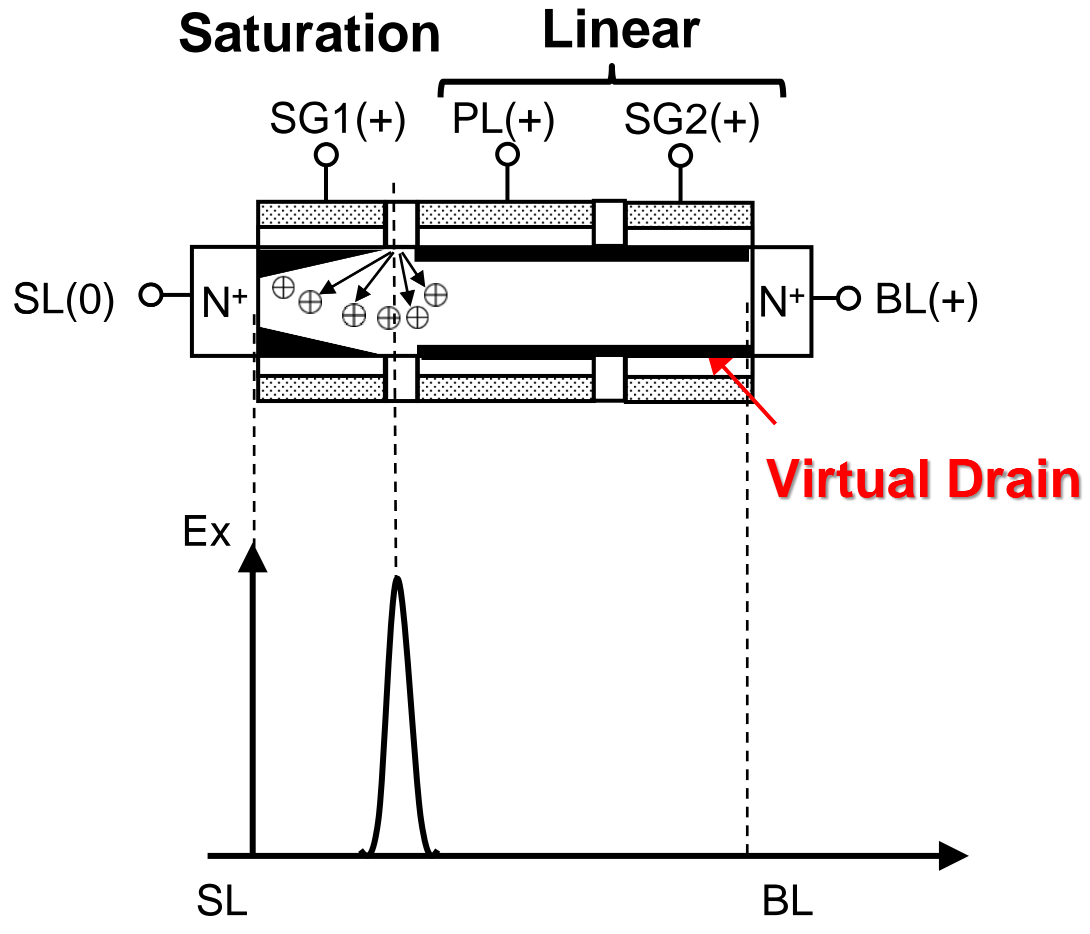


A fixed voltage of 0.8V is applied to PL on reading.

K. Sakui, Y. Li, M. Kakumu, K. Kanazawa, I. Kunishima, Y. Iwata, and N. Harada, "Design Impact on Three Gate Dynamic Flash Memory (3G_DFM) for Long Hole Retention Time and Robust Disturbance Shield," in *Memories - Materials, Devices, Circuits and Systems, Elsevier*, 4, 100054, pp.1-5, May 2023.

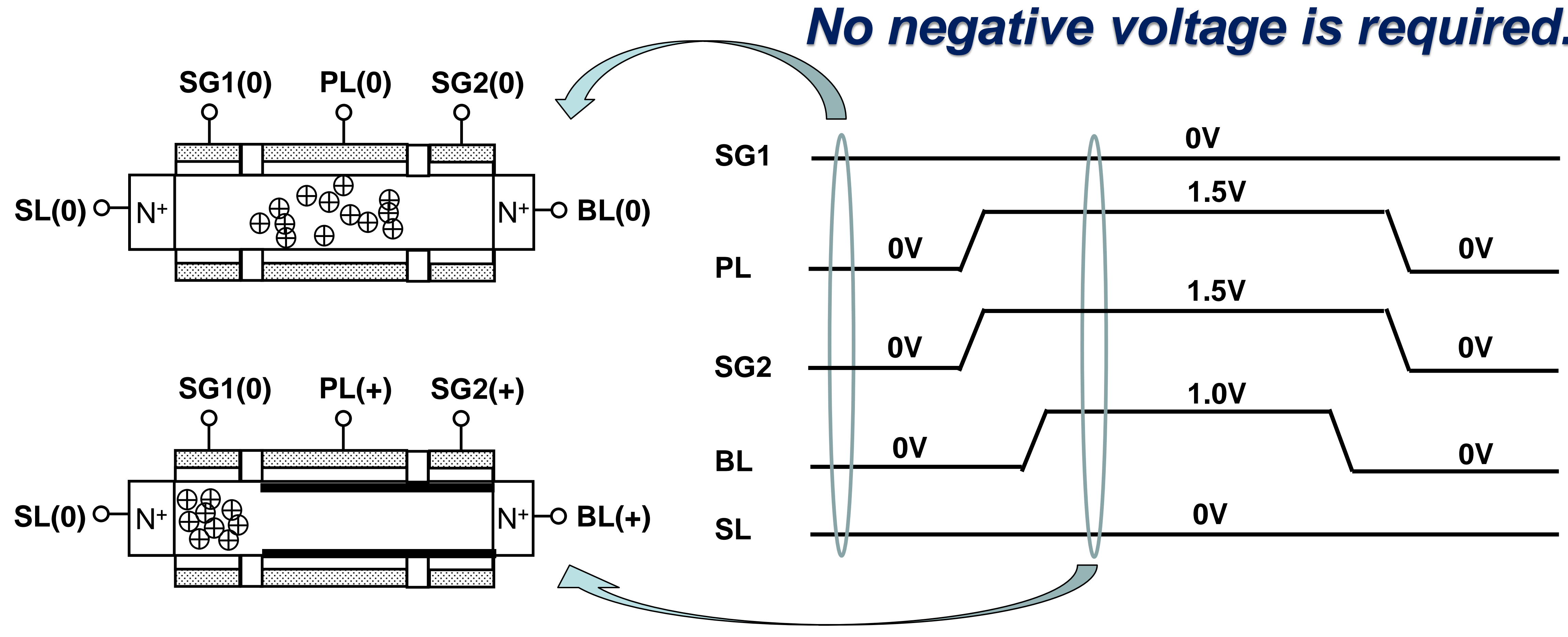
"1" Program Mechanism

~Source-side Impact Ionization~



K. Sakui, Y. Li, M. Kakumu, K. Kanazawa, I. Kunishima, Y. Iwata, and N. Harada, "Design Impact on Three Gate Dynamic Flash Memory (3G_DFM) for Long Hole Retention Time and Robust Disturbance Shield," in *Memories - Materials, Devices, Circuits and Systems, Elsevier*, 4, 100054, pp.1-5, May 2023.

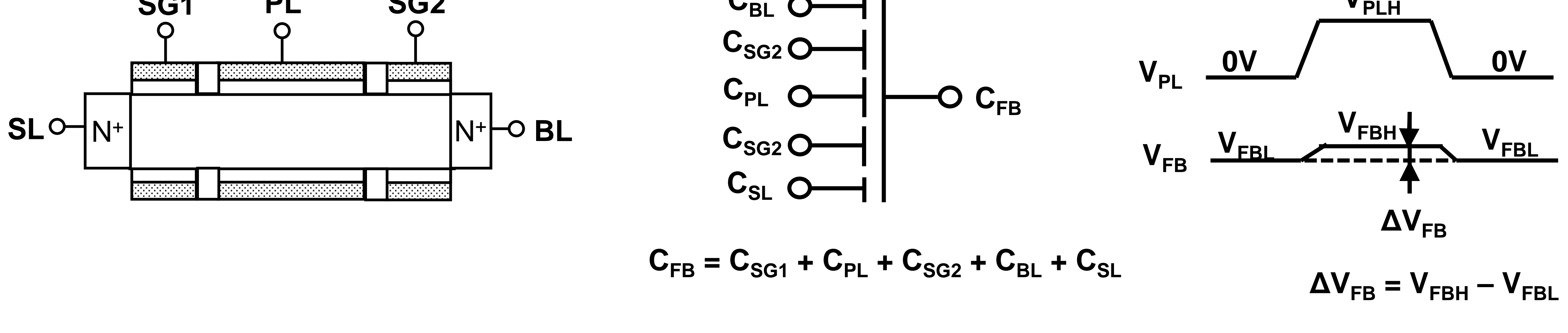
"0" Erase Mechanism



K. Sakui, Y. Li, M. Kakumu, K. Kanazawa, I. Kunishima, Y. Iwata, and N. Harada, "Design Impact on Three Gate Dynamic Flash Memory (3G_DFM) for Long Hole Retention Time and Robust Disturbance Shield," in *Memories - Materials, Devices, Circuits and Systems, Elsevier*, 4, 100054, pp.1-5, May 2023.

The FB Stabilization by the 3G (3 Gates)

Small gate capacitive coupling to FB !



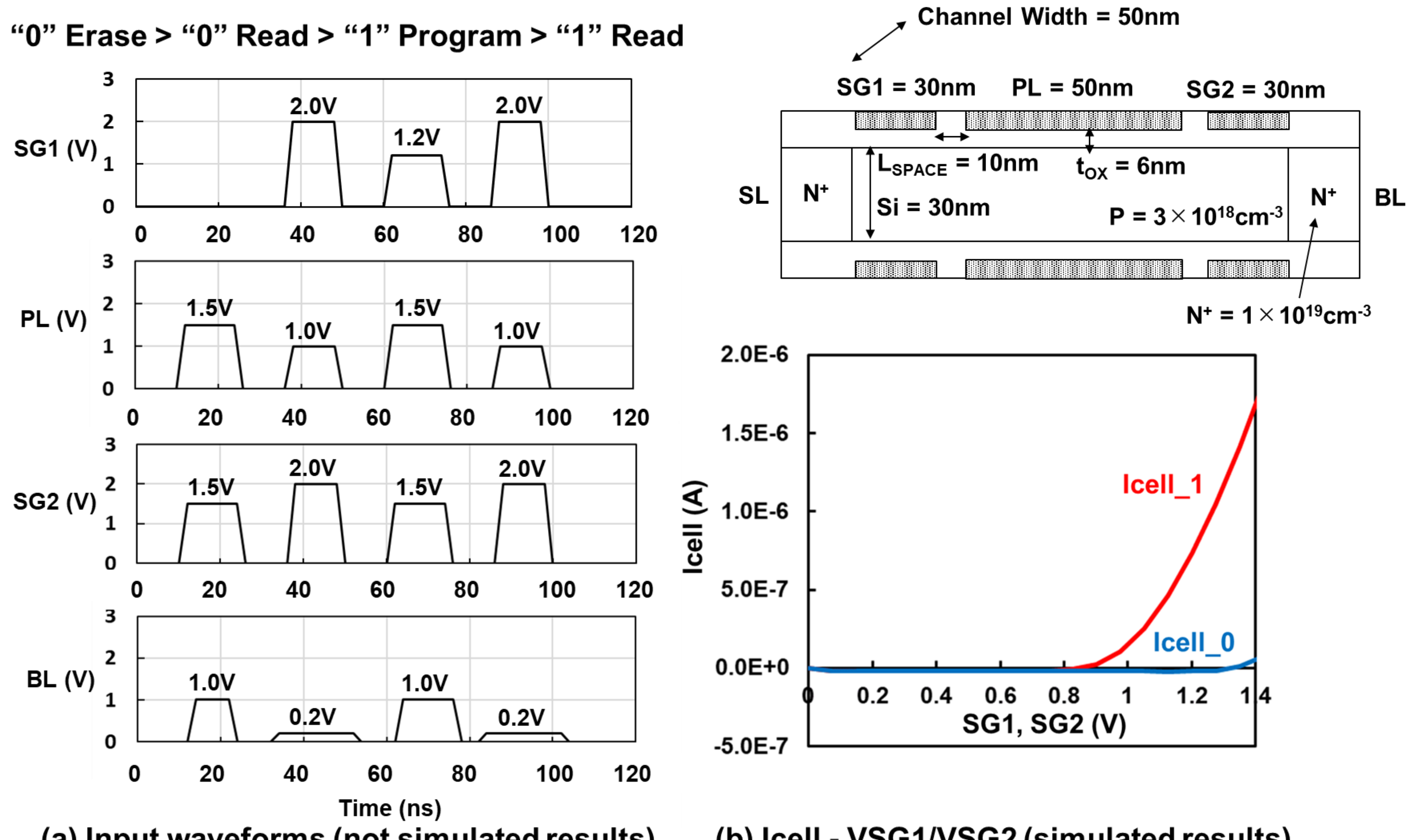
$$\beta_{PL} = \frac{C_{PL}}{C_{SG1} + C_{PL} + C_{SG2} + C_{BL} + C_{SL}} \Rightarrow \text{Small } \beta_{PL}$$

$$= \underline{\underline{\beta_{PL} \times V_{LPH}}}$$

Small

1. K. Sakui and N. Harada, "Dynamic Flash Memory with Dual Gate Surrounding Gate Transistor (SGT)," in *Proc. IEEE IMW*, pp.72-75, May 2021.
2. K. Sakui, Y. Li, M. Kakumu, K. Kanazawa, I. Kunishima, Y. Iwata, and N. Harada, "Design Impact on Three Gate Dynamic Flash Memory (3G_DFM) for Long Hole Retention Time and Robust Disturbance Shield," in *Memories - Materials, Devices, Circuits and Systems, Elsevier*, 4, 100054, pp.1-5, May 2023.

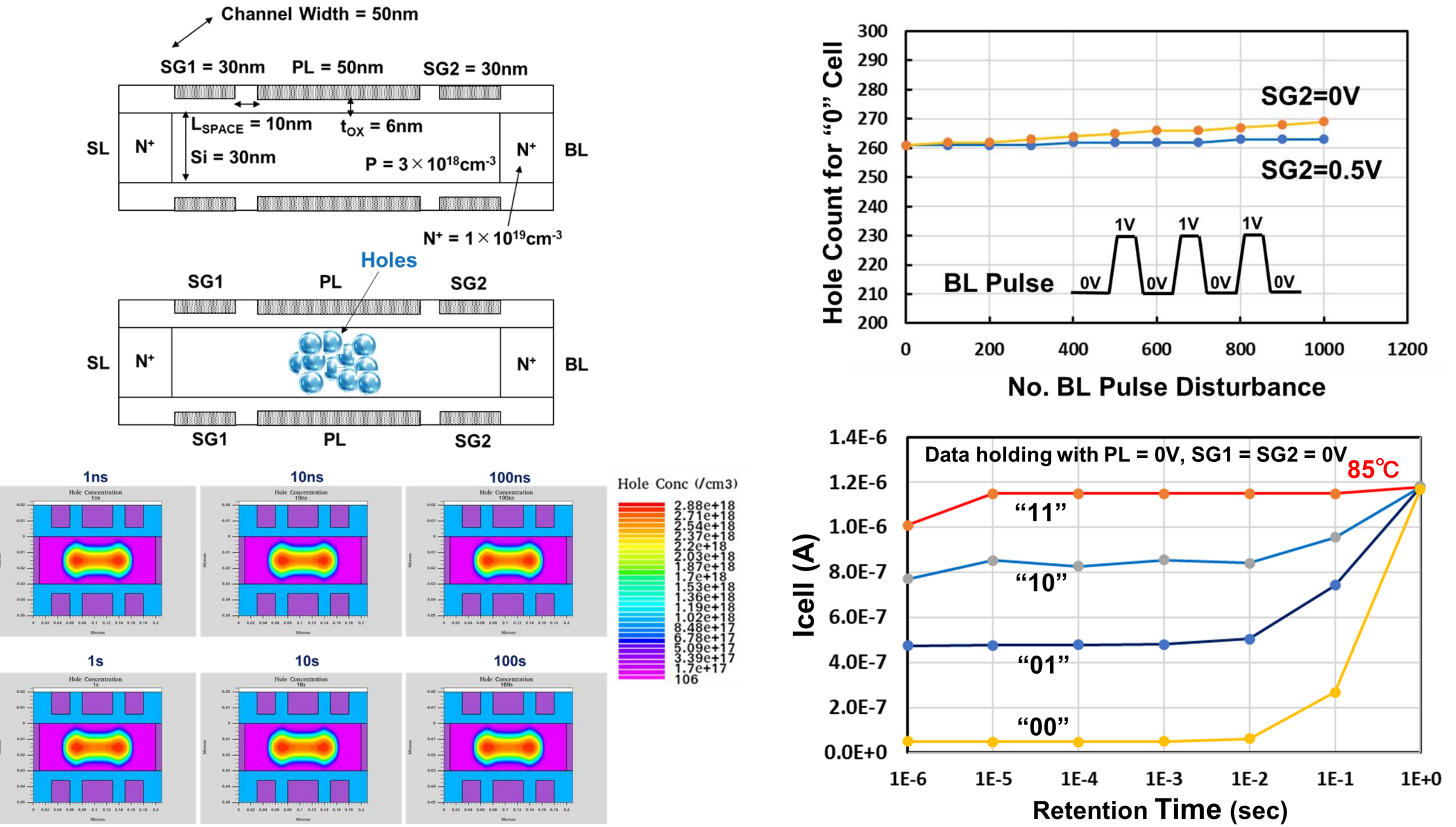
3G DFM Simulation Result



(a) Input waveforms (not simulated results) (b) Icell - VSG1/VSG2 (simulated results)

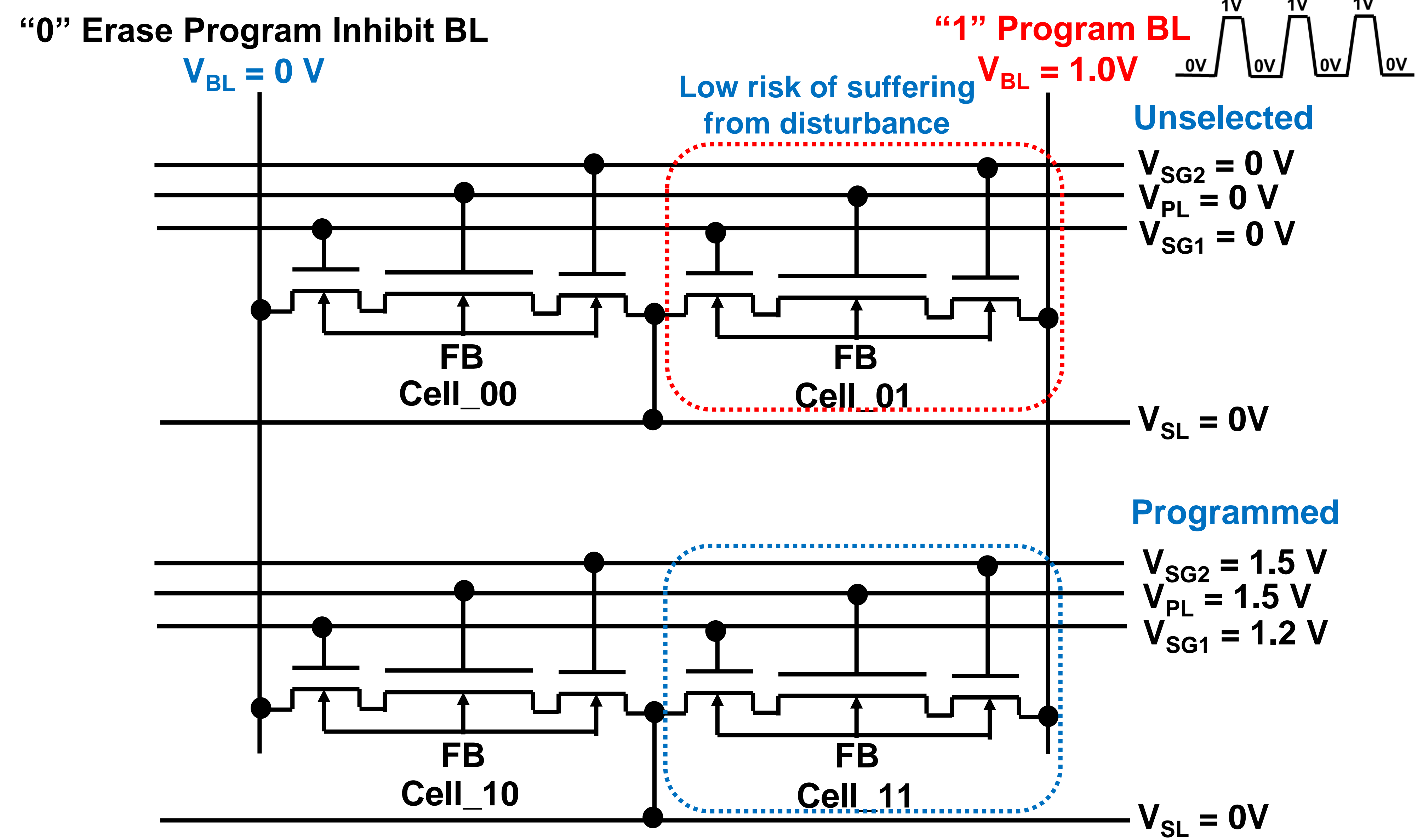
K. Sakui, Y. Li, M. Kakumu, K. Kanazawa, I. Kunishima, Y. Iwata, and N. Harada, "Design Impact on Three Gate Dynamic Flash Memory (3G_DFM) for Long Hole Retention Time and Robust Disturbance Shield," in *Memories - Materials, Devices, Circuits and Systems, Elsevier*, 4, 100054, pp.1-5, May 2023.

2 bit/cell 3G DFM Retention and Cycling



K. Sakui, Y. Li, Y. Iwata, M. Kakumu, and N. Harada, "2 bit/cell Dynamic Flash Memory with Three Gates," in *SSDM*, PS-2-20, Sep. 2023.

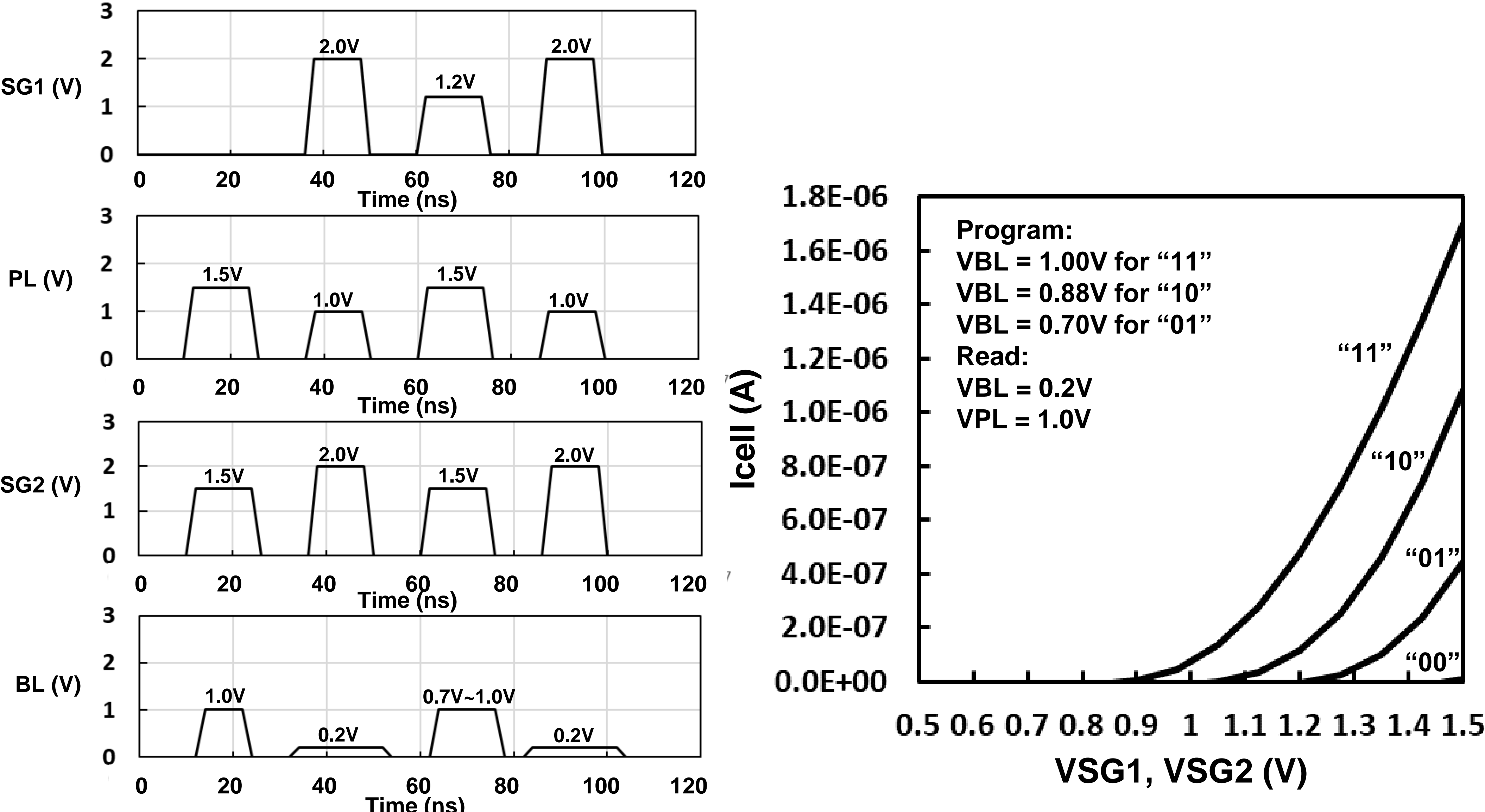
Robust Architecture against Disturbance



K. Sakui, Y. Li, Y. Iwata, M. Kakumu, and N. Harada, "2 bit/cell Dynamic Flash Memory with Three Gates," in *SSDM*, PS-2-20, Sep. 2023.

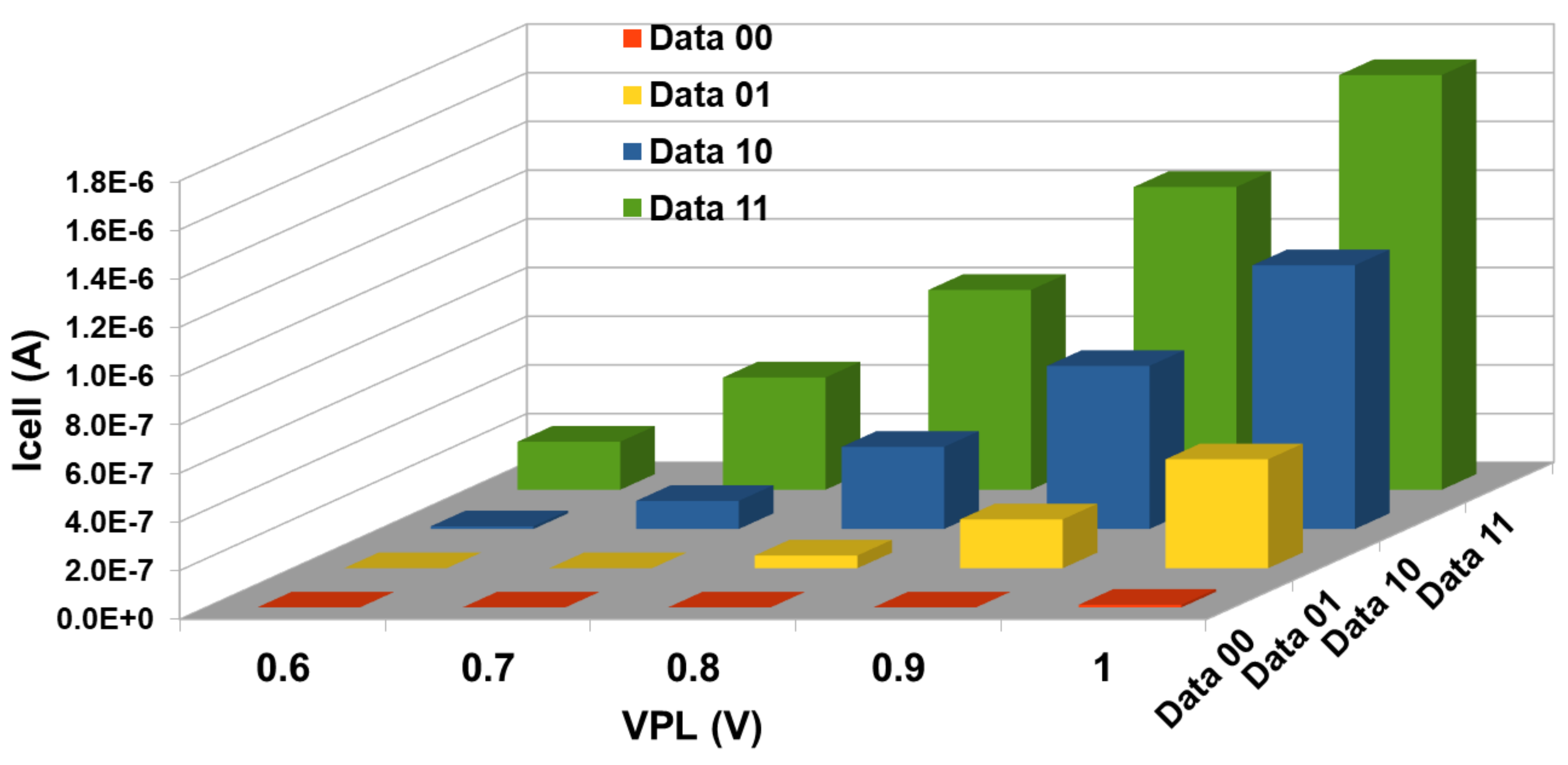
2 bit/cell 3G DFM Standard Operation

"0" Erase > "0" Read > "1" Program > "1" Read



K. Sakui, Y. Li, Y. Iwata, M. Kakumu, and N. Harada, "2 bit/cell Dynamic Flash Memory with Three Gates," in *SSDM*, PS-2-20, Sep. 2023.

2 bit/cell Read by increasing *VPL* voltages

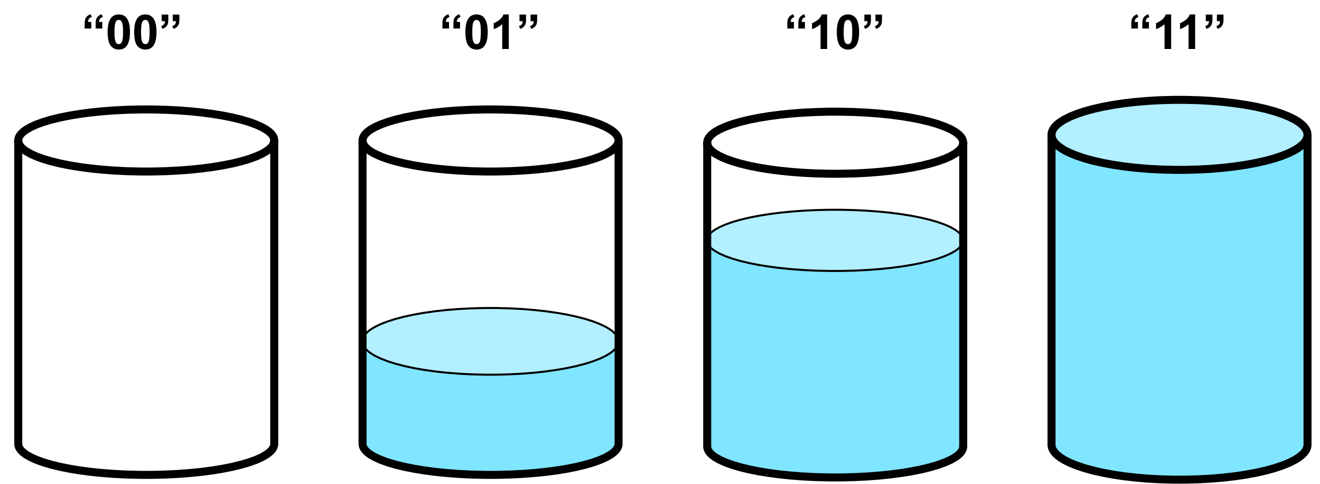


K. Sakui, Y. Li, Y. Iwata, M. Kakumu, and N. Harada, "2 bit/cell Dynamic Flash Memory with Three Gates," in *SSDM*, PS-2-20, Sep. 2023.

Difficulties in realizing MLC DRAM

1. **It is difficult to fulfill a capacitor with four different states.**

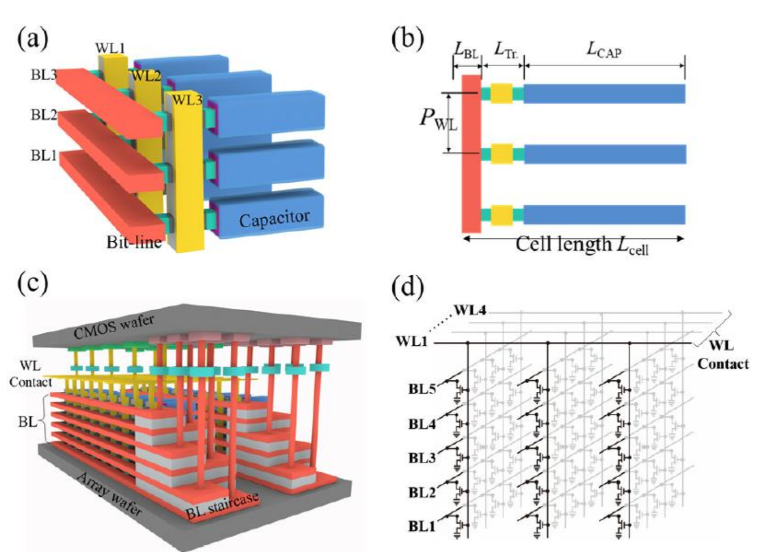
2. ***Bisection Method* cannot be applied for sensing a DRAM cell, because it is *Read Destructive*.**



K. Sakui, Y. Li, Y. Iwata, M. Kakumu, and N. Harada, "2 bit/cell Dynamic Flash Memory with Three Gates," in *SSDM*, PS-2-20, Sep. 2023.

3D DRAM Papers

CXMT: Stacked 1T1C
IMW 2023C



M. Huang et al., "A 3D Stackable 1T1C DRAM: Architecture, Process Integration and Circuit Simulation," in *Proc. IEEE IMW*, pp.29-32, May 2023.

Samsung: Stacked 1T1C
VLSI 2023

Double Gate

Hor. WL

Capacitor

Ver. BL

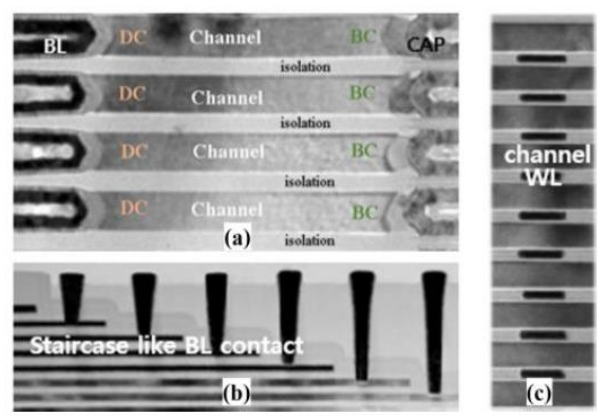
(a)

Double Gate

Hor. BL

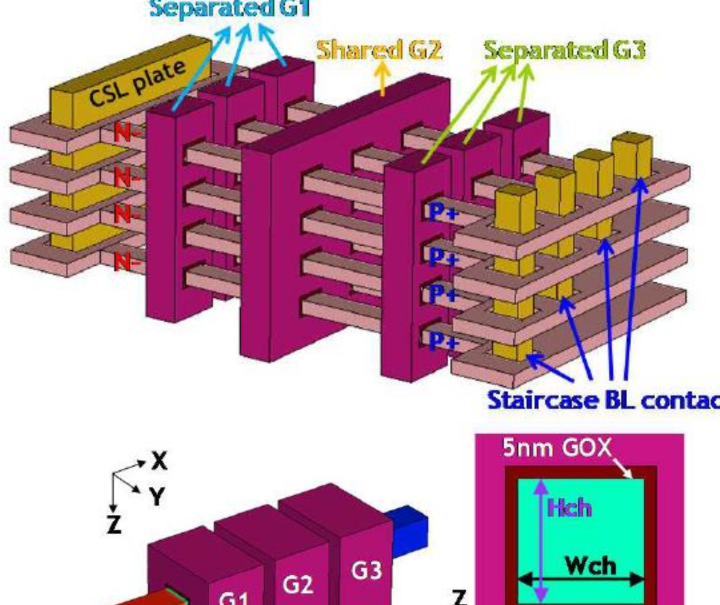
Ver. WL

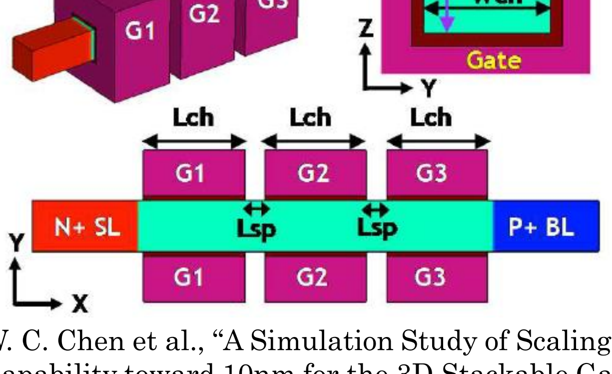
(b)



J.W. Han et al., "Ongoing Evolution of DRAM Scaling via Third Dimension - Vertically Stacked DRAM -," in *2023 Symposium on VLSI Technology and Circuits Digest of Technical Papers*, TFS1-1, pp.1-2, Jun. 2023.

Macronix: Stacked Thyristor
IEDM 2022, IMW 2023





W. C. Chen et al., "A Simulation Study of Scaling Capability toward 10nm for the 3D Stackable Gate-Controlled Thyristor (GCT) DRAM Device," in *Proc. IEEE IMW*, pp.25-28, May 2023.

Stacked DFM Features

1. Low-cost volatile memory can be realized by stacking structure.

2. Initial Stacked DFM can start from a much smaller number of tiers than that of Stacked 1T1C DRAM.

3. Like 3D NAND, Stacked DFM has a potential to continue development for increasing density.

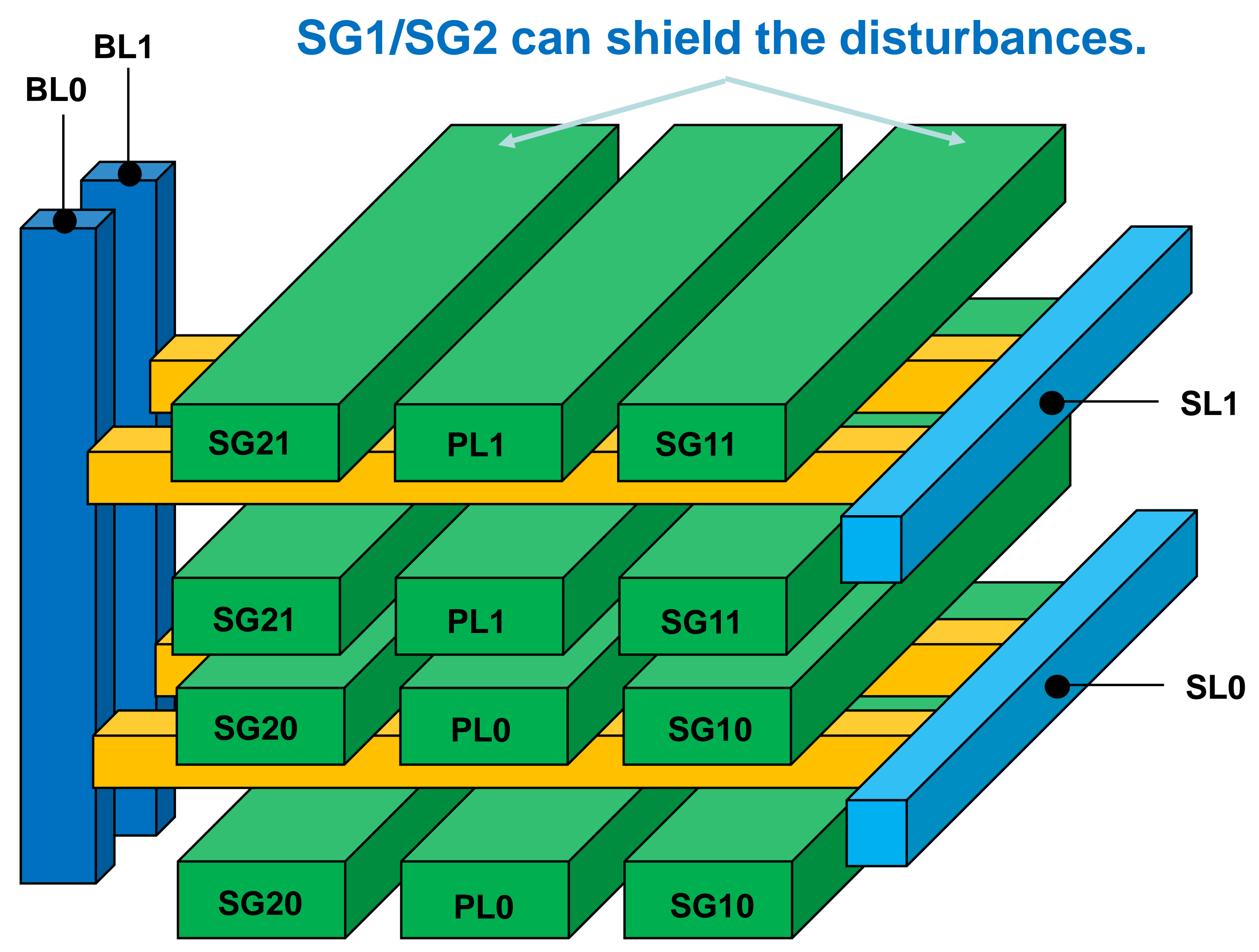
4. Robust structures against disturbance: 1) 3 gate structure, 2) BL shield architecture, 3) Shielded gate structure.

5. The process technology for the cell transistor of Stacked 1T1C DRAM can be utilized for the development of Stacked DFM.

6. Stacked DFM can be fabricated with the conventional Si process.

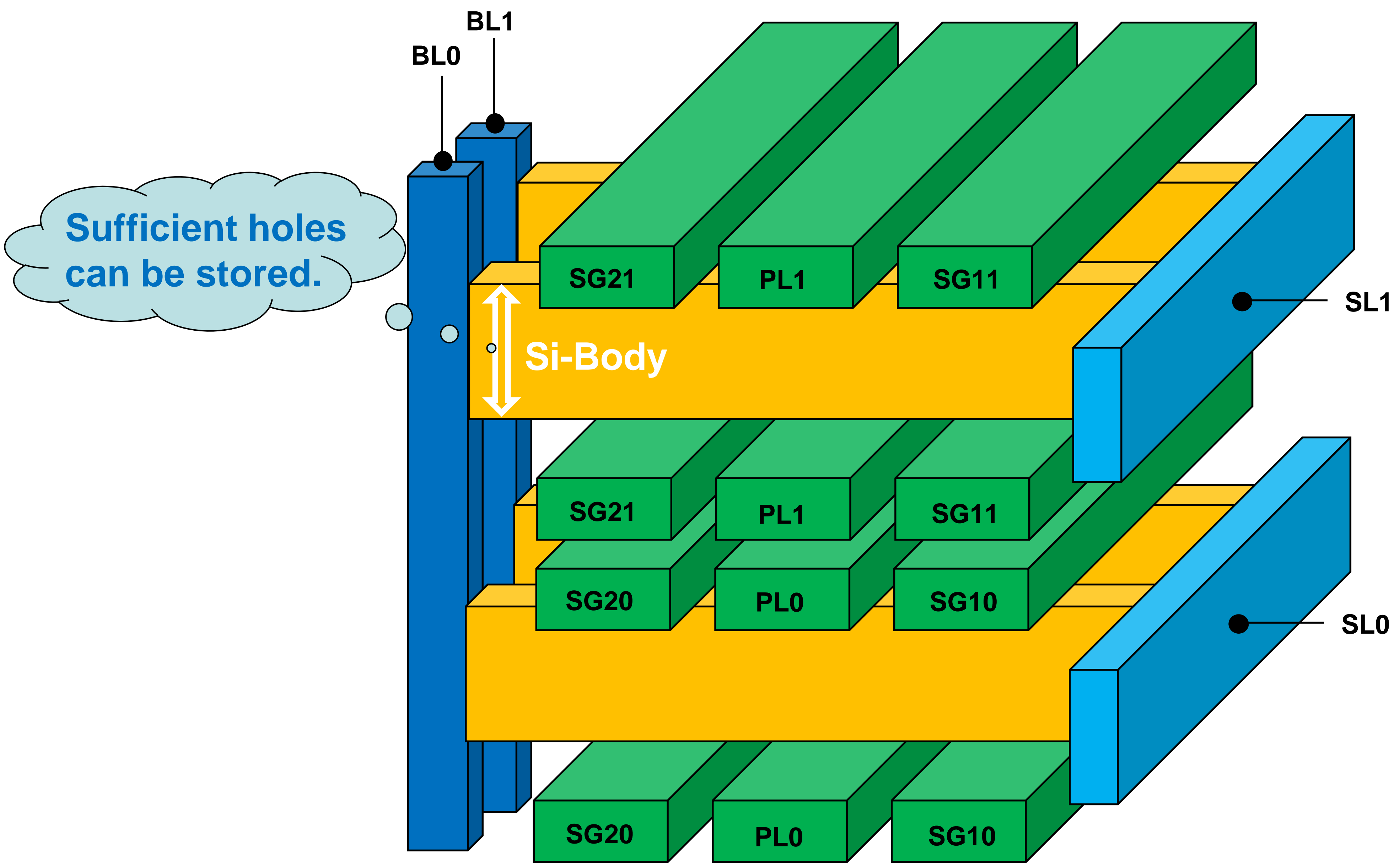
Double Gate Stacked DFM (Horizontal Gates)

SG1/SG2 can shield the disturbances.



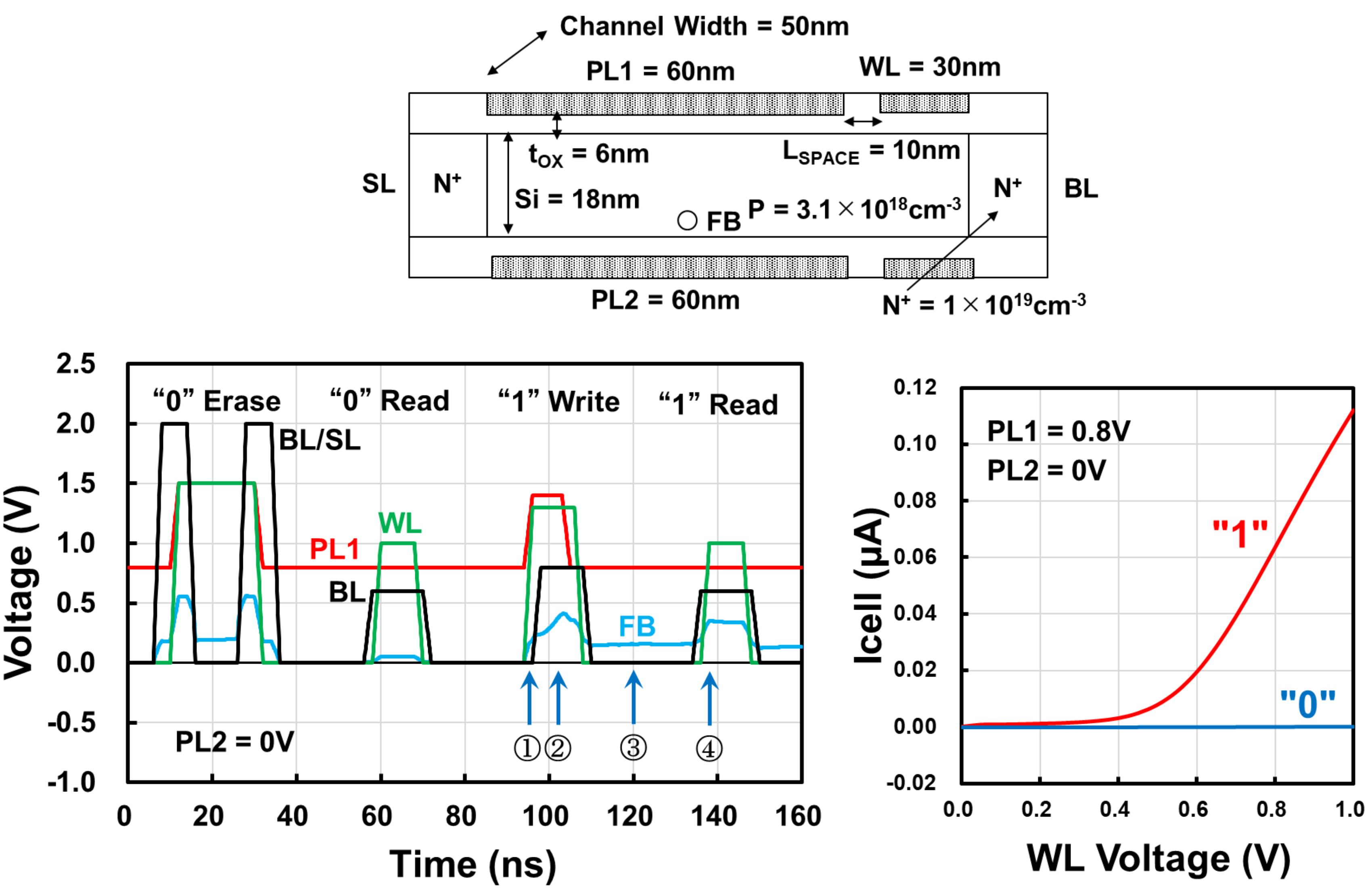
K. Sakui, Y. Li, M. Kakumu, and Nozomu Harada, “Stacked Dynamic Flash Memory (DFM) for a High Density Memory,” *2023 Flash Memory Summit*, Aug. 2023.

Si-Body Thickness Control without Cell Size Increase



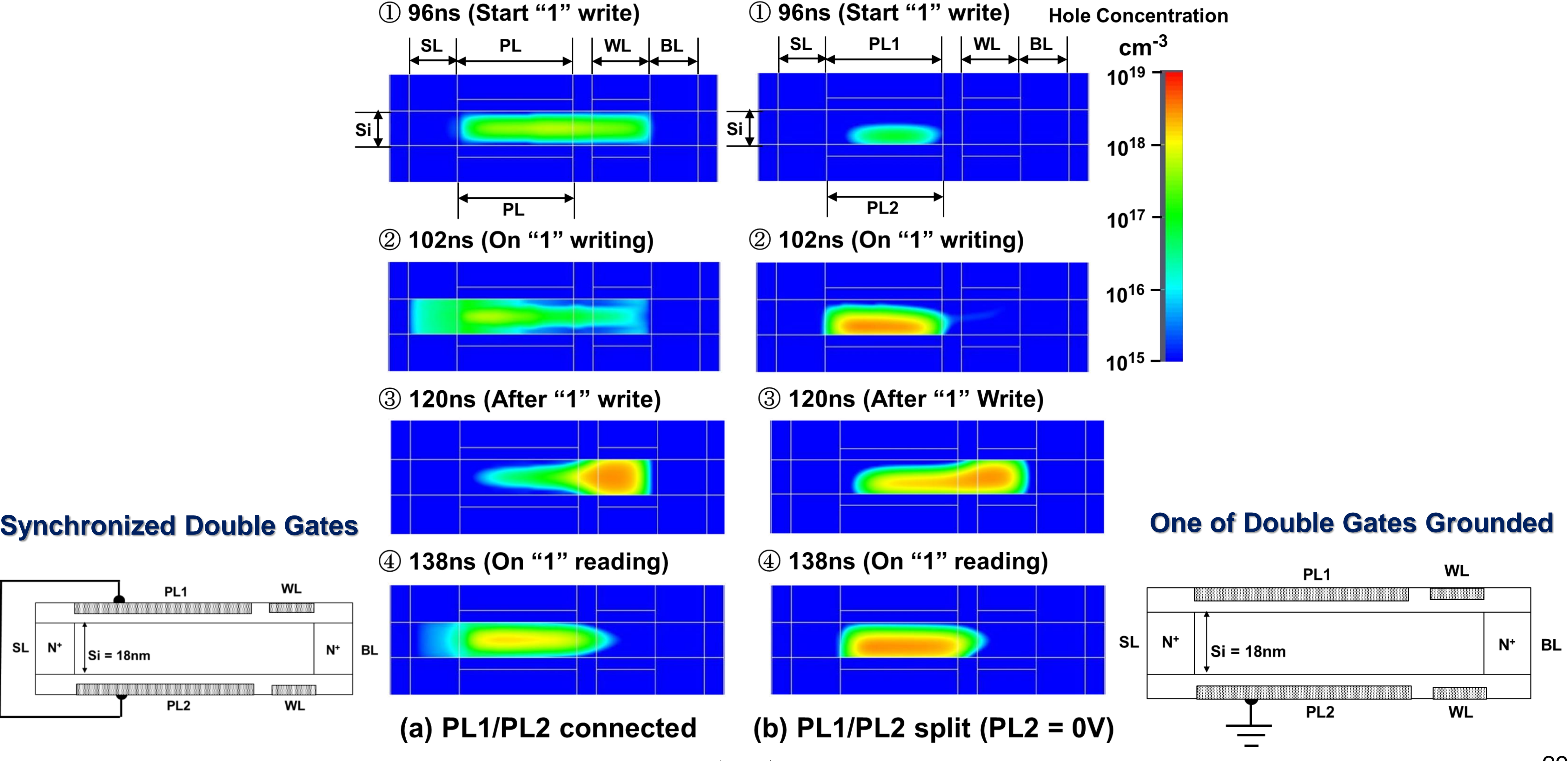
K. Sakui, Y. Li, M. Kakumu, and Nozomu Harada, "Stacked Dynamic Flash Memory (DFM) for a High Density Memory," *2023 Flash Memory Summit*, Aug. 2023.

Double Gate 2G DFM Simulation Result



K. Sakui and N. Harada, "Read Non-Destructive Dynamic Flash Memory (DFM) with Dual and Double Gates," in *SSDM*, F-4-02, pp.405-406, Sep. 2022.

Hole Concentration: (a) PL1 = PL2, (b) PL2 = 0V

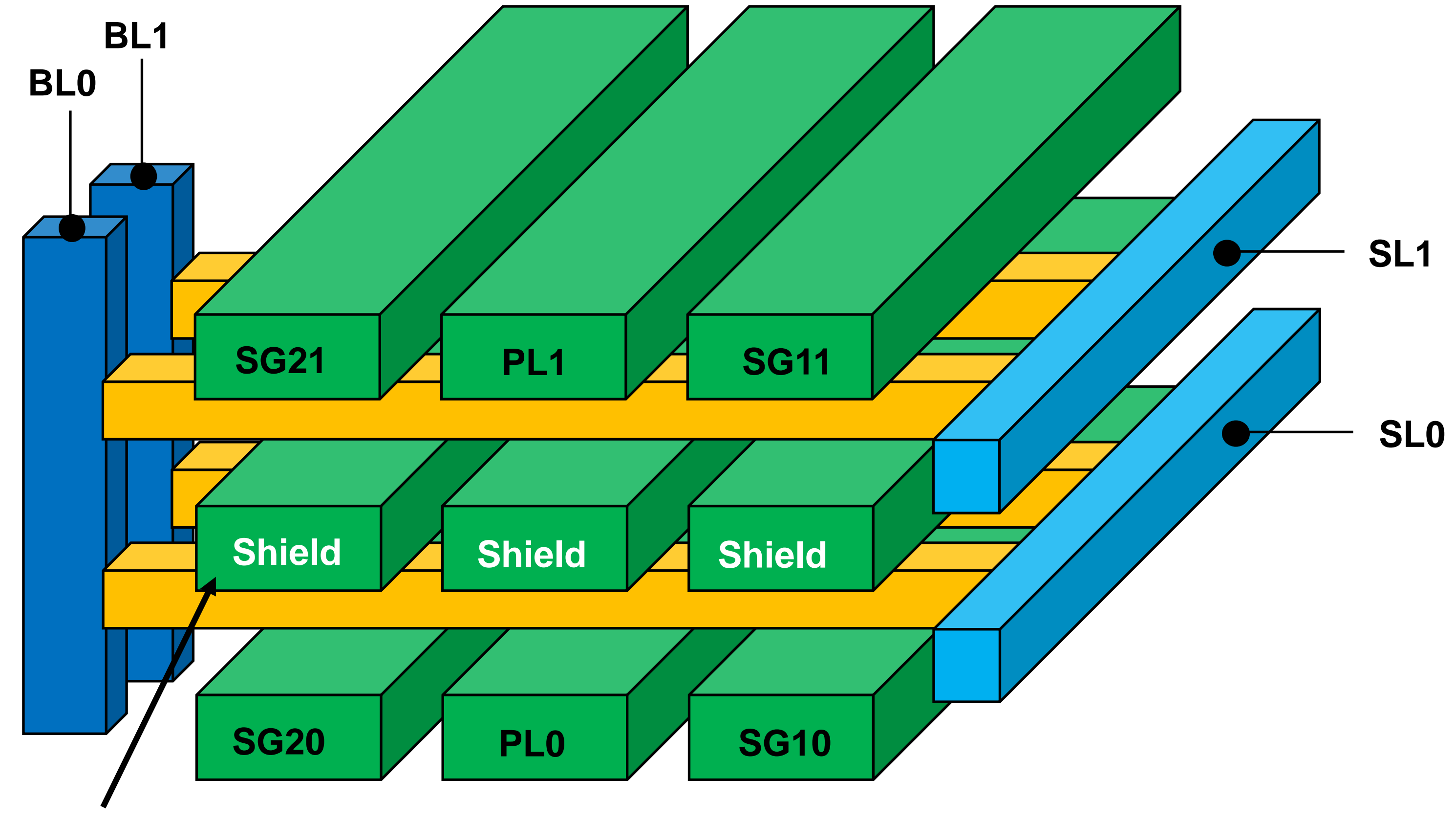


(a) PL1/PL2 connected

(b) PL1/PL2 split (PL2 = 0V)

K. Sakui and N. Harada, "Read Non-Destructive Dynamic Flash Memory (DFM) with Dual and Double Gates," in *SSDM*, F-4-02, pp.405-406, Sep. 2022.

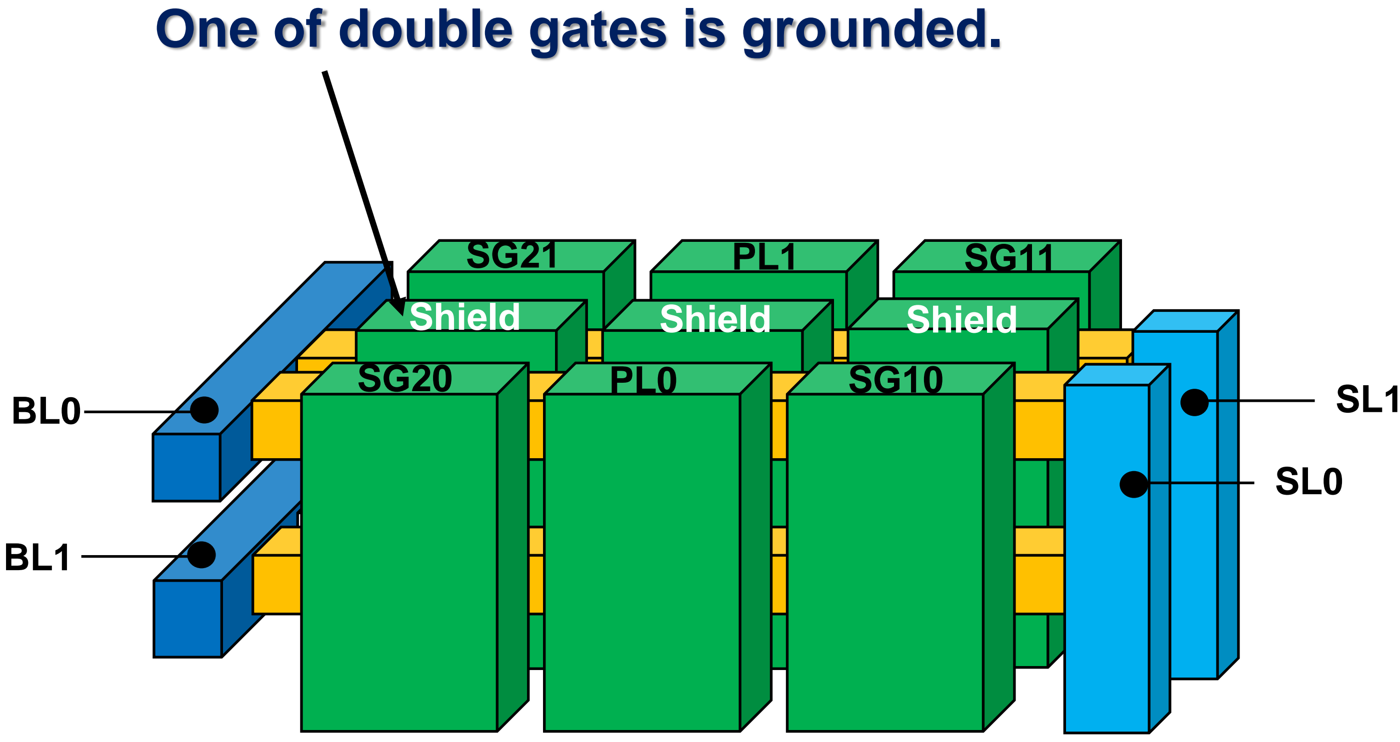
Grounded Double Gate Stacked DFM (Horizontal Gate)



One of double gates is grounded.

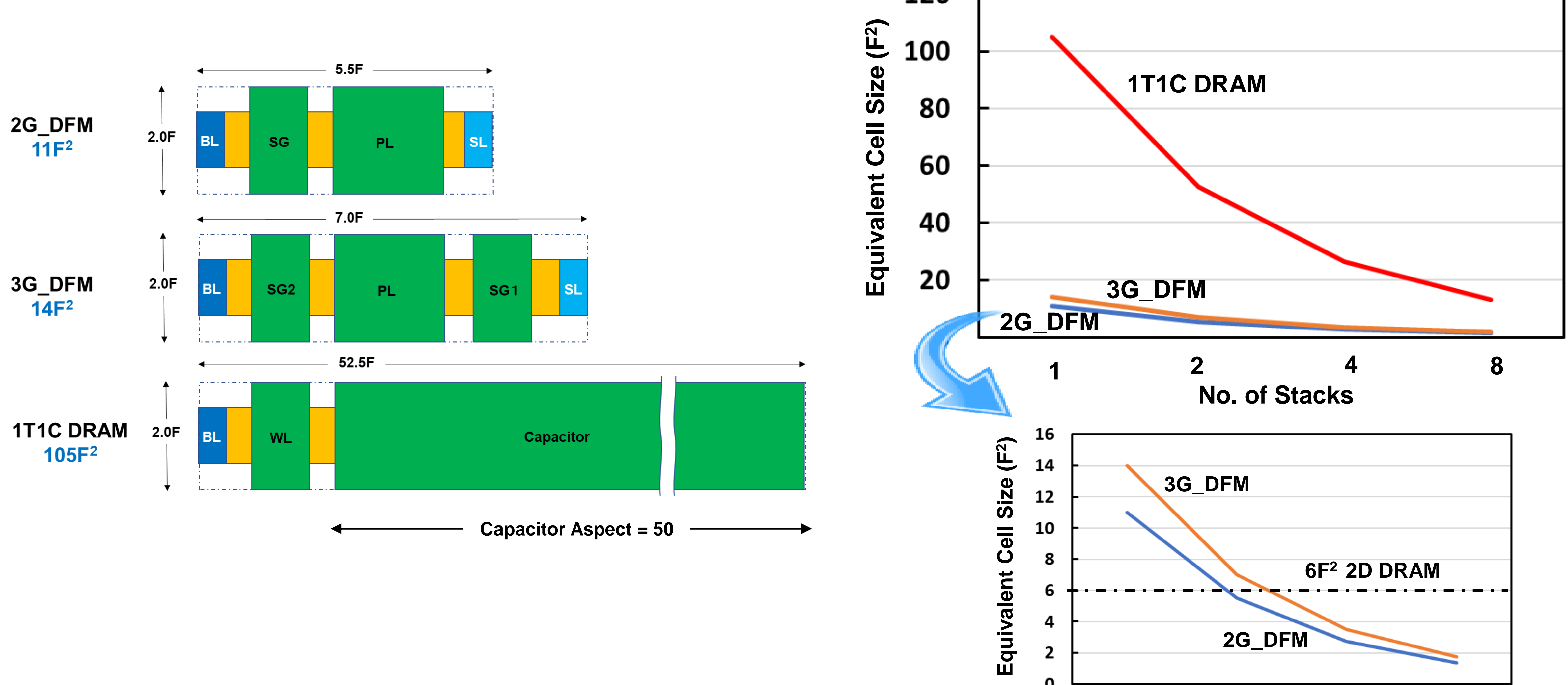
K. Sakui, Y. Li, M. Kakumu, and Nozomu Harada, "Stacked Dynamic Flash Memory (DFM) for a High Density Memory," *2023 Flash Memory Summit*, Aug. 2023.

Grounded Double Gate Stacked DFM (Vertical Gate)



K. Sakui, Y. Li, M. Kakumu, and Nozomu Harada, "Stacked Dynamic Flash Memory (DFM) for a High Density Memory," *2023 Flash Memory Summit*, Aug. 2023.

Horizontal Gate Structure Equivalent Cell Size

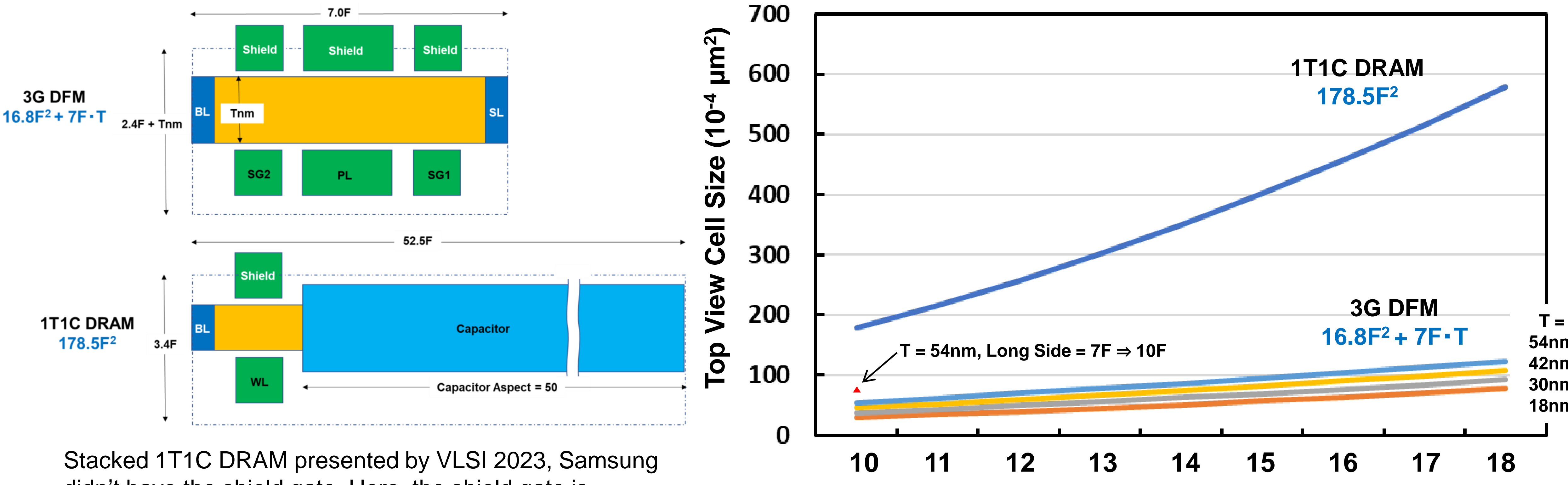


K. Sakui, Y. Li, M. Kakumu, and Nozomu Harada, "Stacked Dynamic Flash Memory (DFM) for a High Density Memory," *2023 Flash Memory Summit*, Aug. 2023.

Vertical Gate Structure (Without Stair VIA Connection Area)

The FB Si thickness (T) is validated at T=18nm by TCAD.

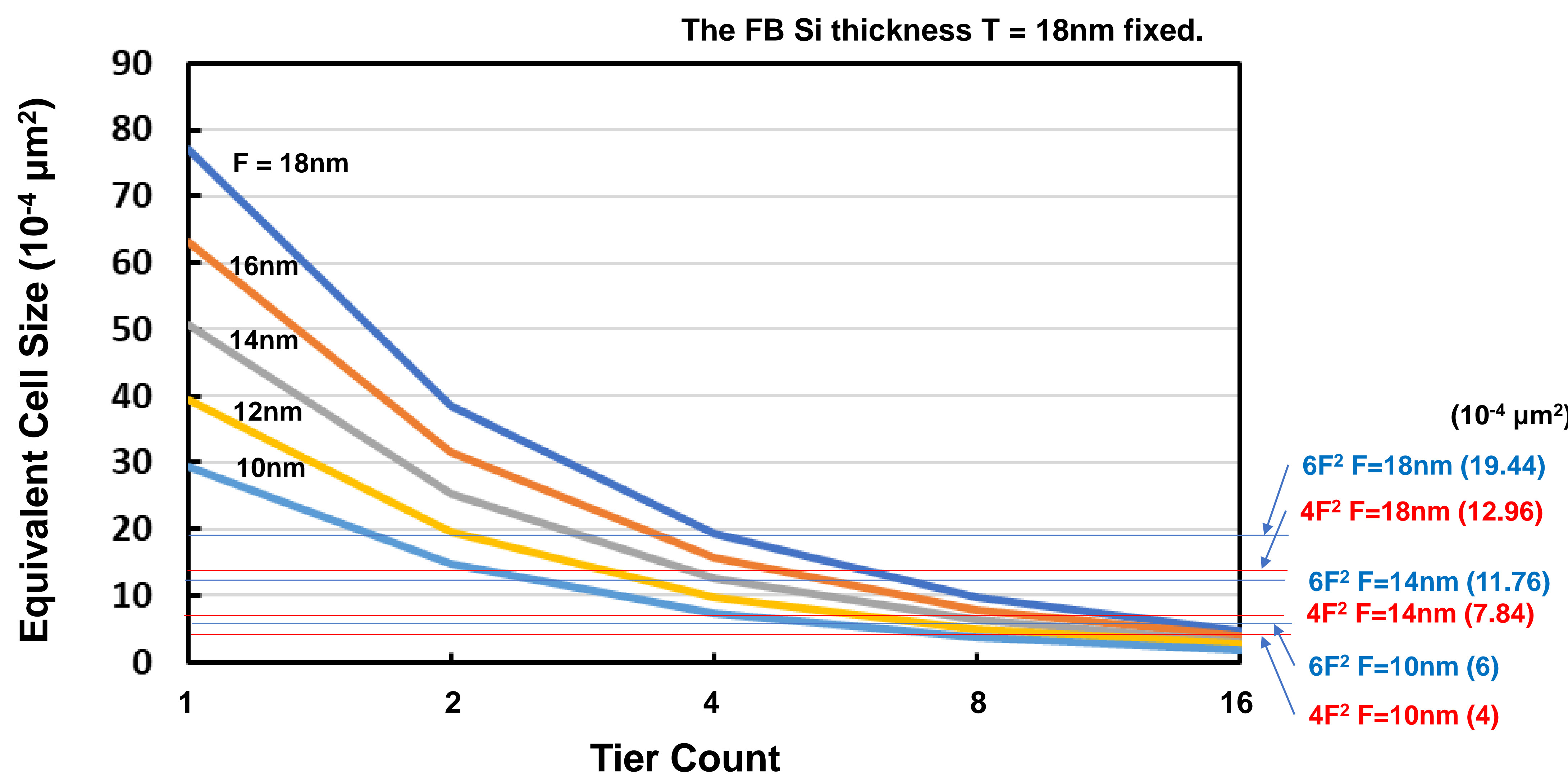
K. Sakui and N. Harada, "Read Non-Destructive Dynamic Flash Memory (DFM) with Dual and Double Gates," in *SSDM*, F-4-02, pp.405-406, Sep. 2022.



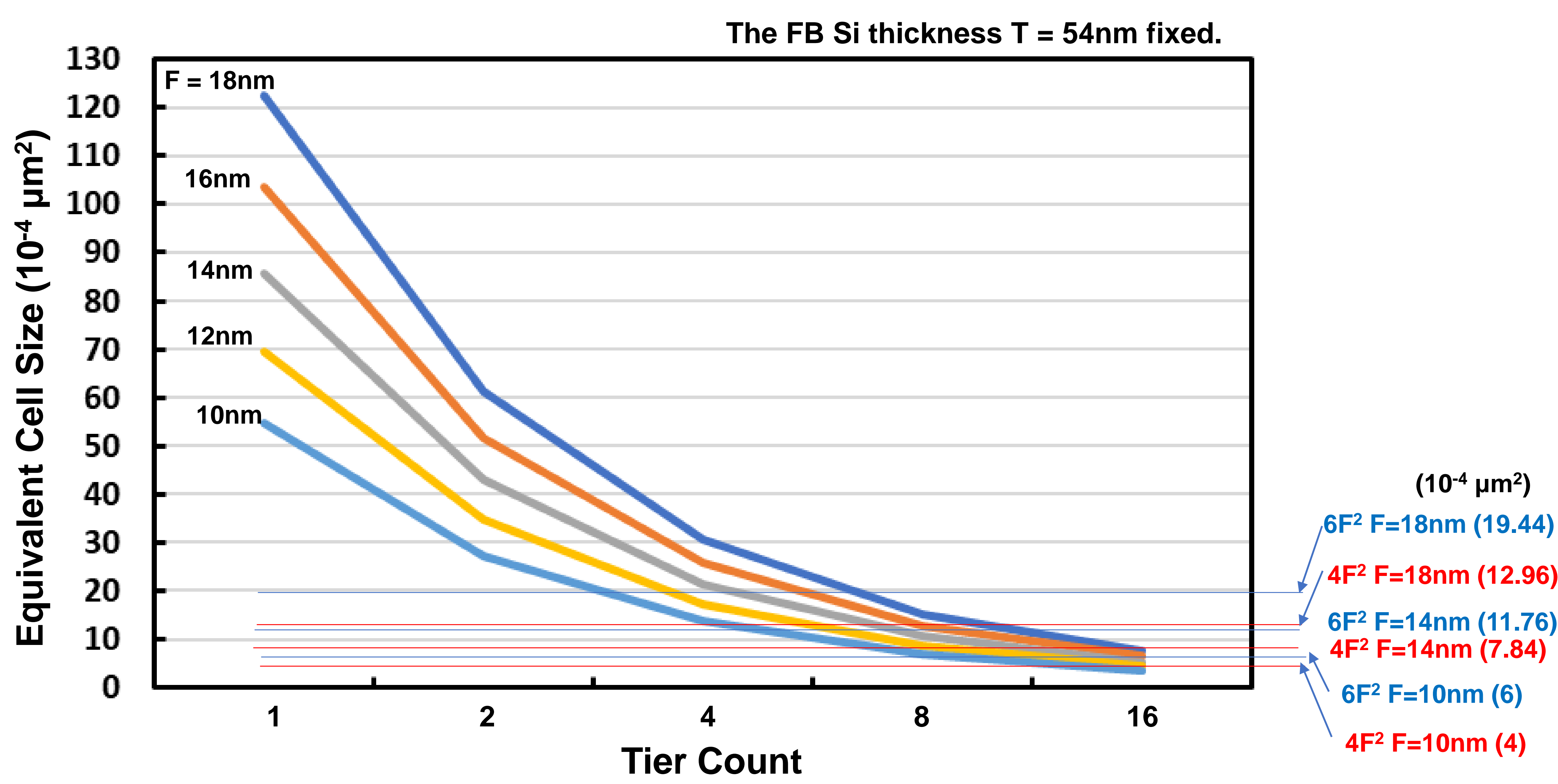
Stacked 1T1C DRAM presented by VLSI 2023, Samsung didn't have the shield gate. Here, the shield gate is considered, because it can shirink the cell size.

The FB Si thickness (T) of Stacked 3G DFM is 18nm/30nm/42nm/54nm fixed.

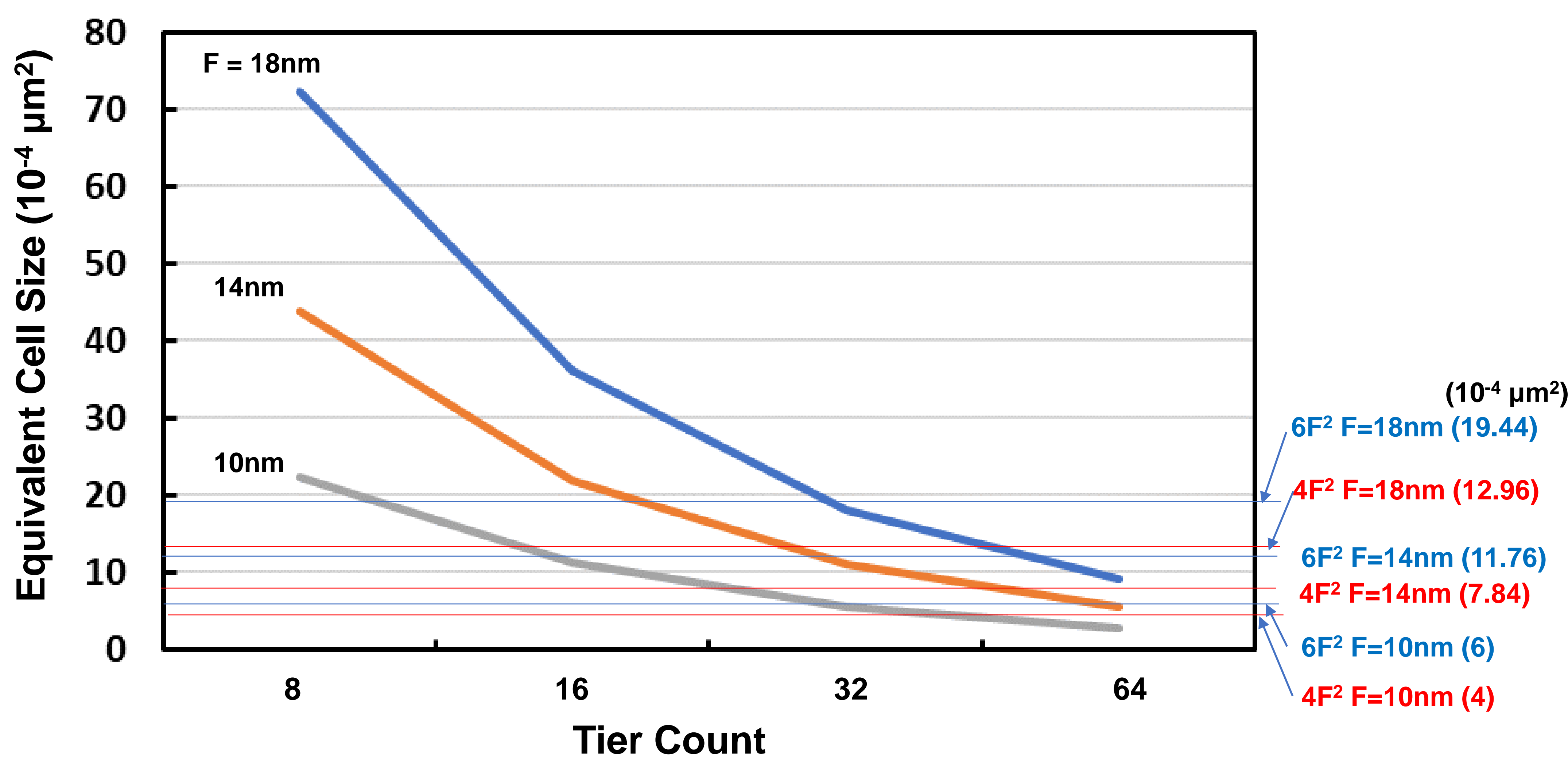
Horizontal Gate Stacked DFM Equivalent Cell Size (Without Stair VIA Connection Area)



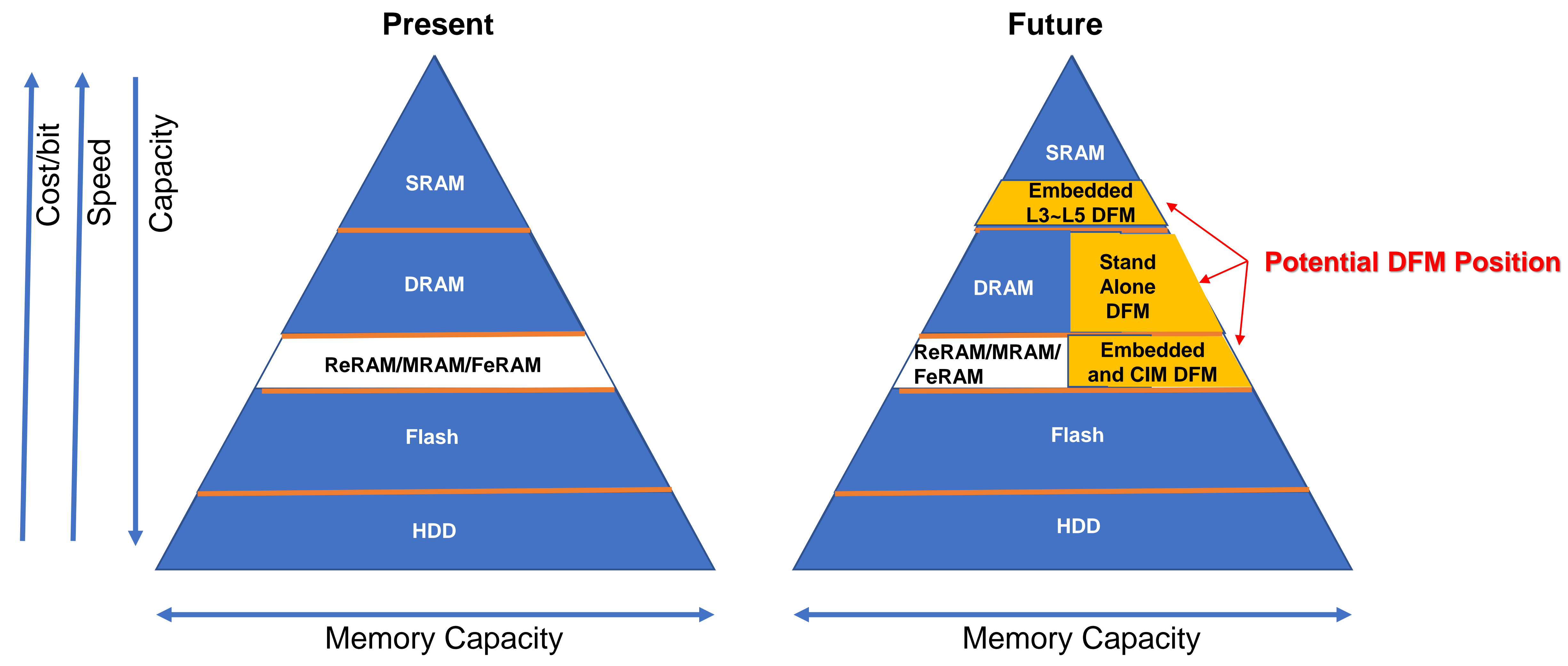
Horizontal Gate Stacked DFM Equivalent Cell Size (Without Stair VIA Connection Area)



Horizontal Gate Stacked 1T1C DRAM Equivalent Cell Size (Without Stair VIA Connection Area)



Potential DFM Position



K. Sakui, Y. Li, M. Kakumu, and Nozomu Harada, "Stacked Dynamic Flash Memory (DFM) for a High Density Memory," *2023 Flash Memory Summit*, Aug. 2023.

DFM Conclusion

1. The 2bit/cell 3G DFM has been proposed by controlling the number of holes in the FB.

2. The stacked 3G DFM has a substantial potential to realize a much smaller equivalent cell than $6F^2$ with 3~4 tiers.

3. Unlike emerging memories, such as ReRAM and MRAM, neither variable resistors nor special materials are needed. It should be noted that DFM can be fabricated with the conventional Si process.

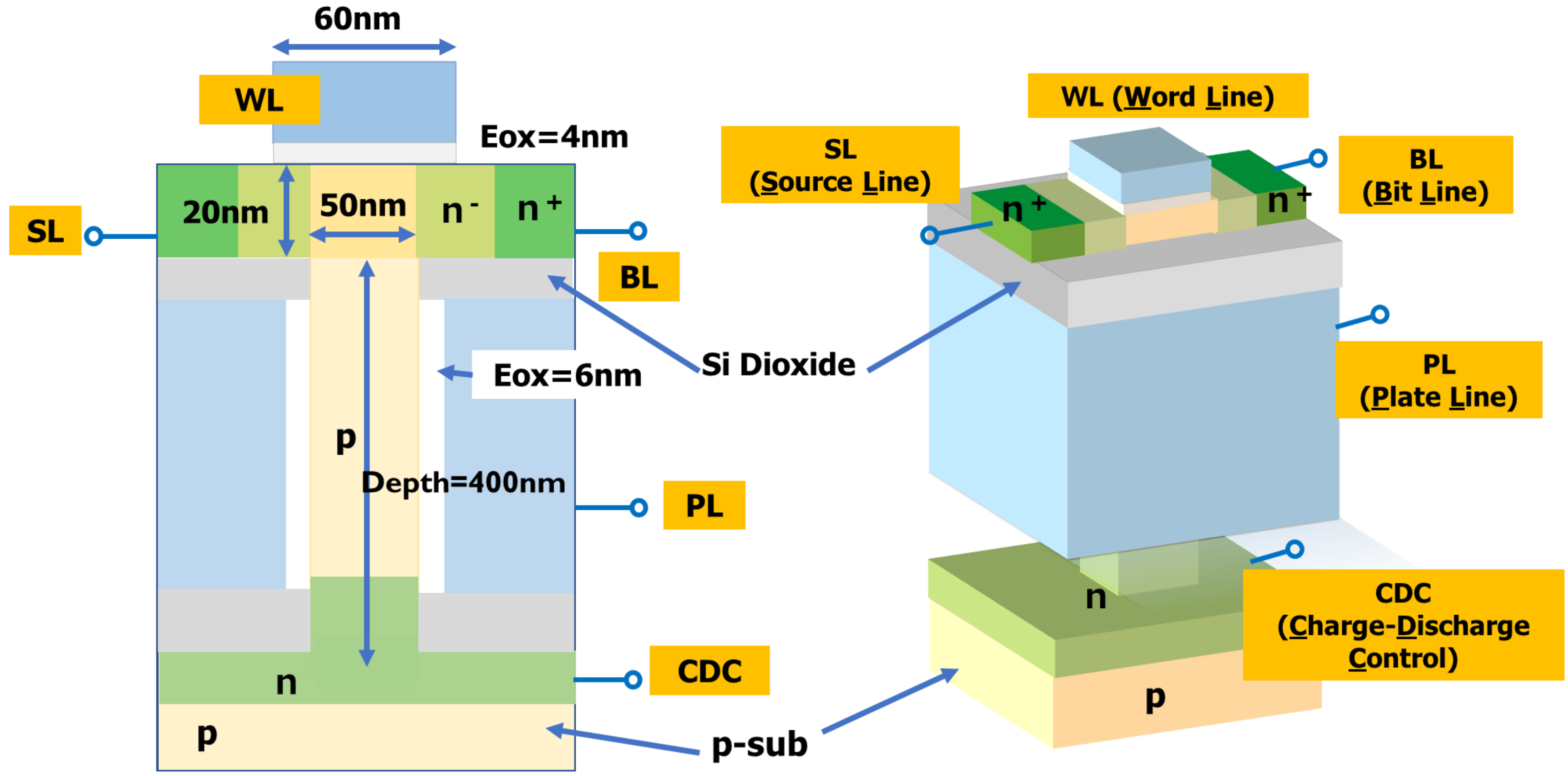
4. A low cost stackable DFM is a promising device positioned next to DRAM and NAND in the memory hierarchy.

Agenda

1. DFM: Dynamic Flash Memory
2. **KFBM: Key shape Floating Body Memory**
3. SGT: Surrounding Gate Transistor
4. BBCube: Bumpless Build Cube

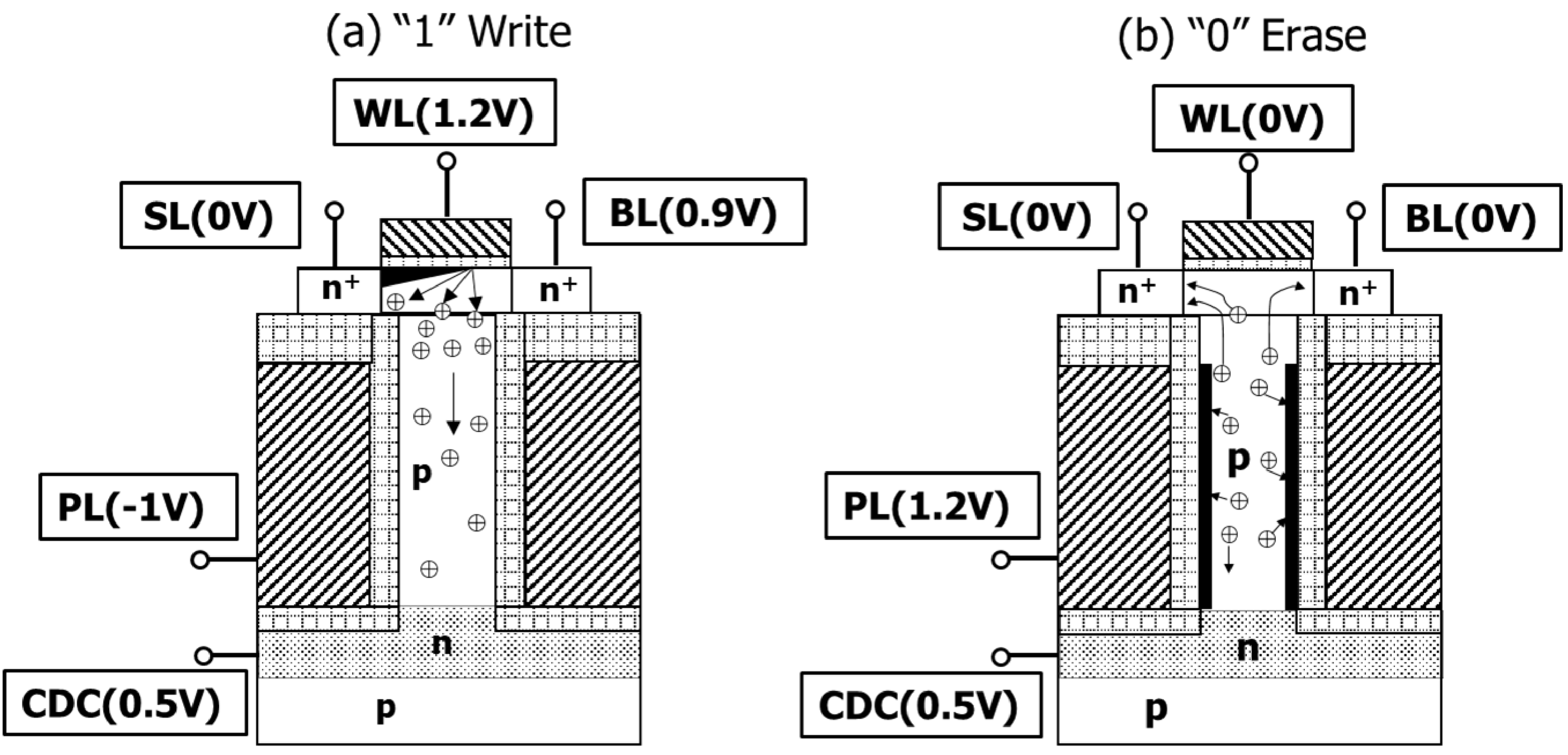
39

KFBM (Key shape Floating Body Memory) Structure



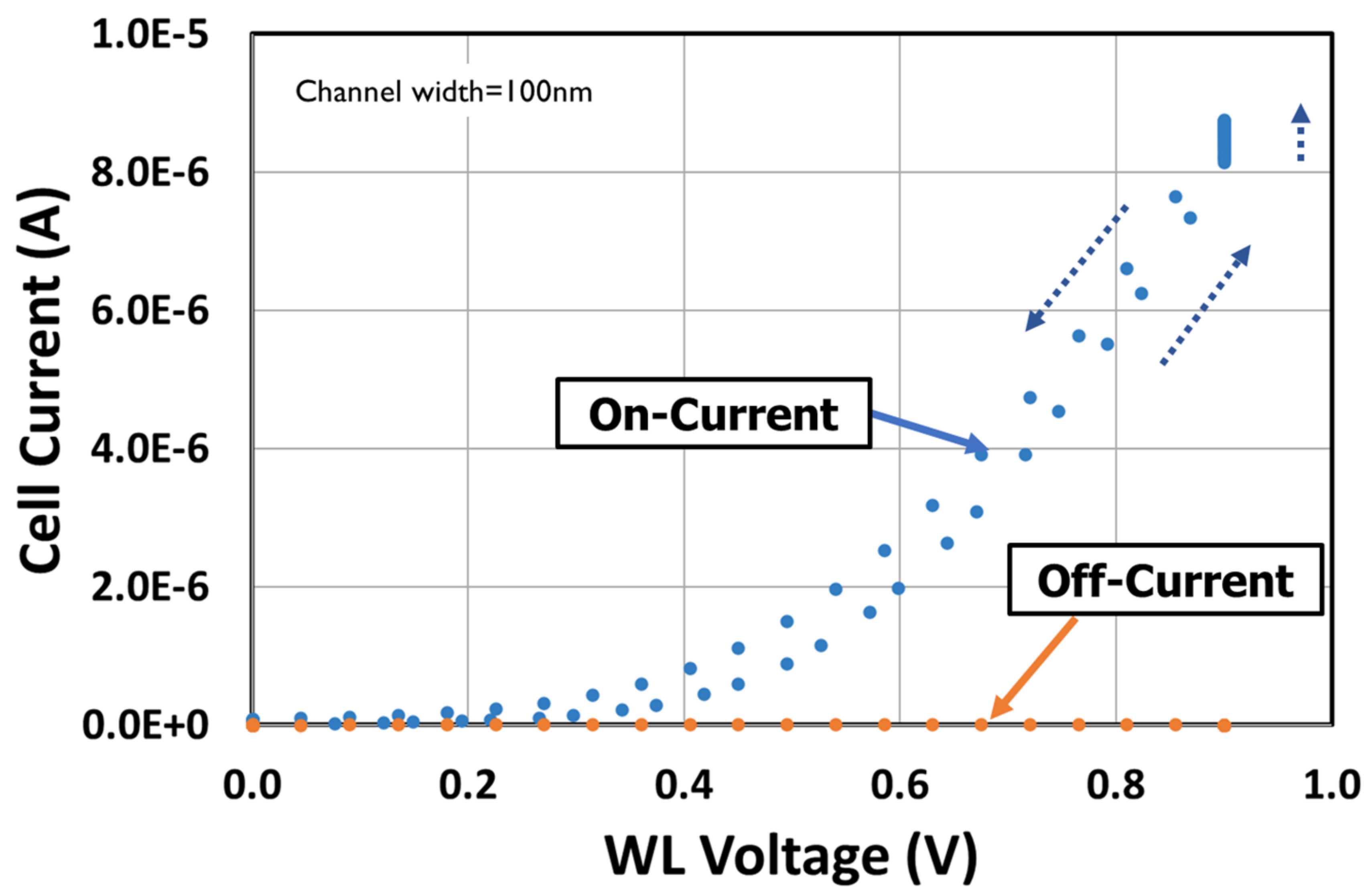
M. Kakumu, Y. Li, K. Sakui, and N. Harada, "Fully bulk CMOS compatible Key Shape Floating Body Memory (KFBM)," in *Memories - Materials, Devices, Circuits and Systems, Elsevier*, 4, 100061, pp.1-5, May 2023.

On-Off Mechanism of KFBM



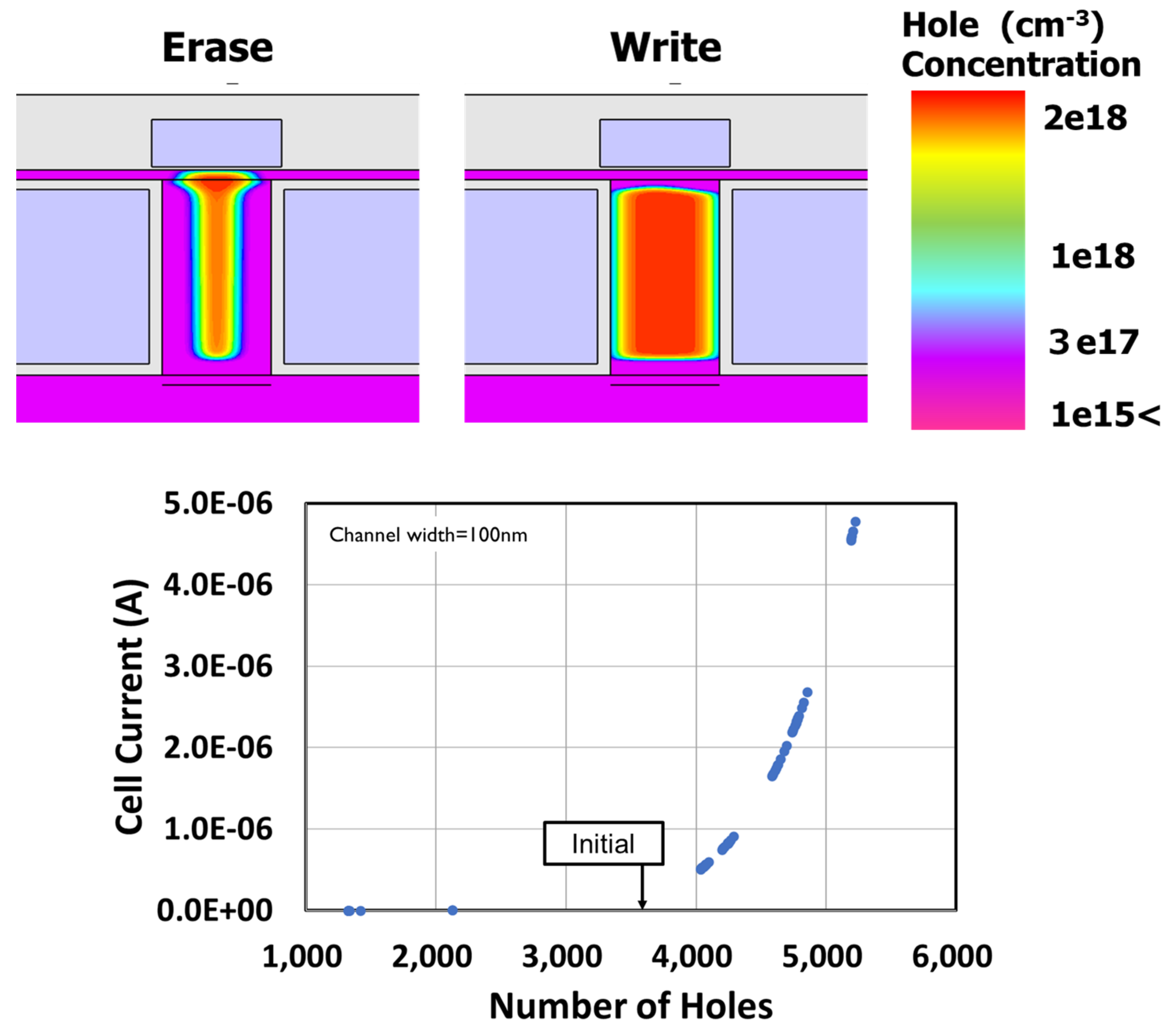
M. Kakumu, Y. Li, K. Sakui, and N. Harada, "Fully bulk CMOS compatible Key Shape Floating Body Memory (KFBM)," in *Memories - Materials, Devices, Circuits and Systems, Elsevier*, 4, 100061, pp.1-5, May 2023.

KFBM On-Off Characteristics



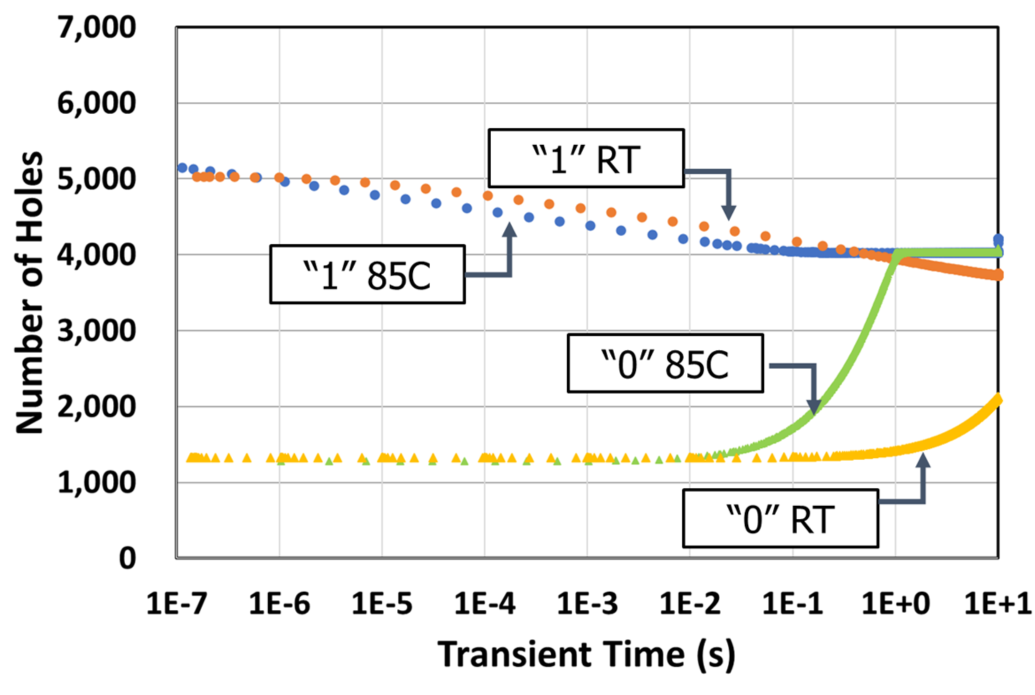
M. Kakumu, Y. Li, K. Sakui, and N. Harada, "Fully bulk CMOS compatible Key Shape Floating Body Memory (KFBM)," in *Memories - Materials, Devices, Circuits and Systems, Elsevier*, 4, 100061, pp.1-5, May 2023.

Hole Number vs. Cell Current

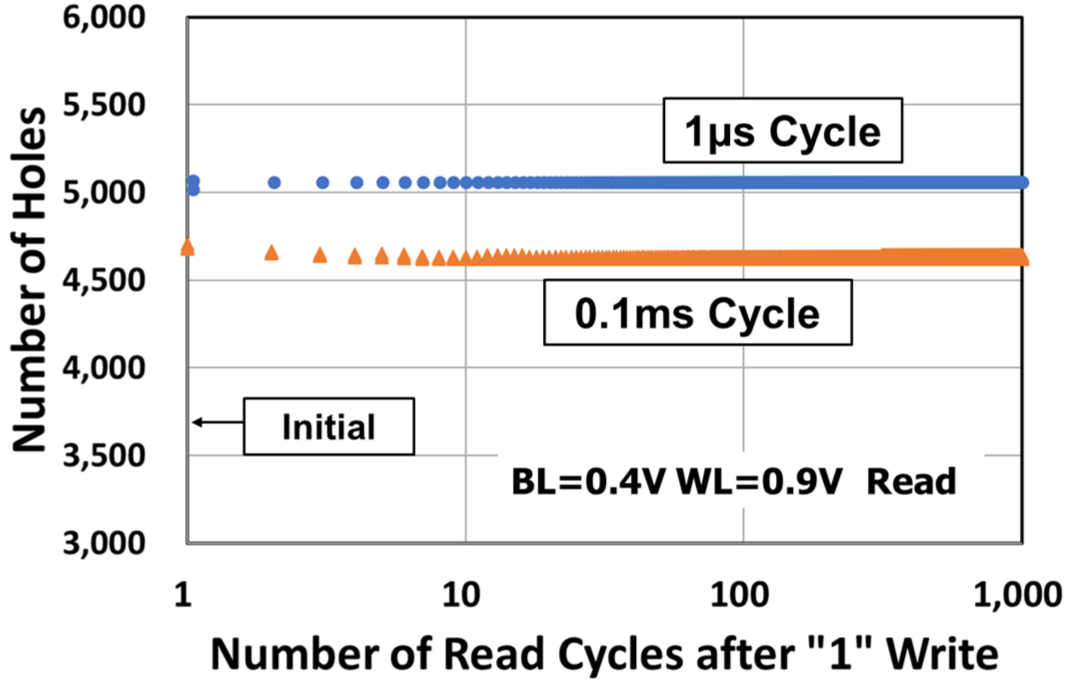


M. Kakumu, Y. Li, K. Sakui, and N. Harada, "Fully bulk CMOS compatible Key Shape Floating Body Memory (KFBM)," in *Memories - Materials, Devices, Circuits and Systems, Elsevier*, 4, 100061, pp.1-5, May 2023.

Retention and Cycling



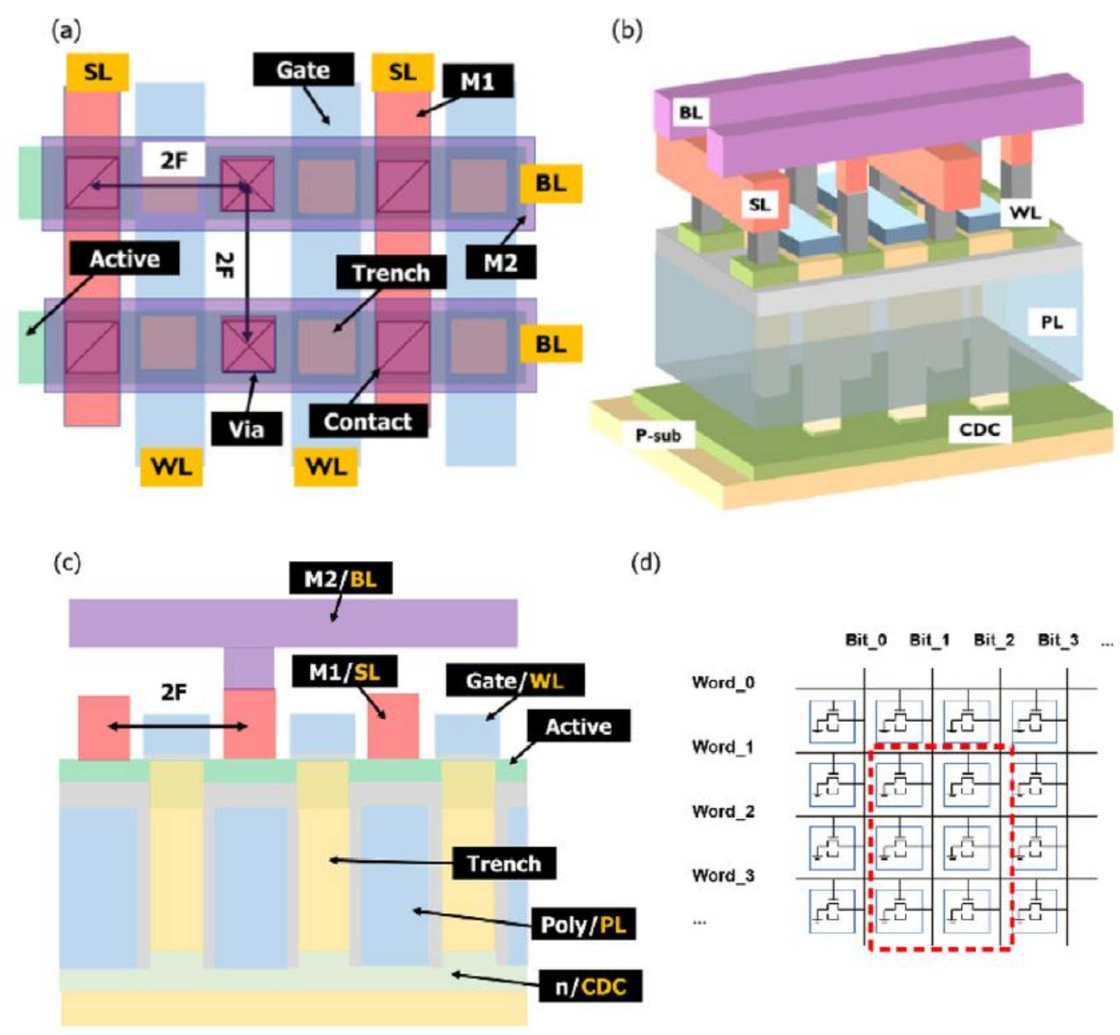
Retention time at 27C (RT) and 85C



Hole number at each periodical read (non-destructive read)

M. Kakumu, Y. Li, K. Sakui, and N. Harada, "Fully bulk CMOS compatible Key Shape Floating Body Memory (KFBM)," in *Memories - Materials, Devices, Circuits and Systems, Elsevier*, 4, 100061, pp.1-5, May 2023.

Fully Compatible Process with Conventional CMOS



M. Kakumu, Y. Li, K. Sakui, and N. Harada, "Fully bulk CMOS compatible Key Shape Floating Body Memory (KFBM)," in *Memories - Materials, Devices, Circuits and Systems, Elsevier*, 4, 100061, pp.1-5, May 2023.

KFBM Conclusion

1. Fully CMOS compatible KFBM has been proposed.

2. KFBM cell consists of MOSFET with virtual floating body formed by bulk silicon and trench with on/off margins of more than three orders of magnitude.

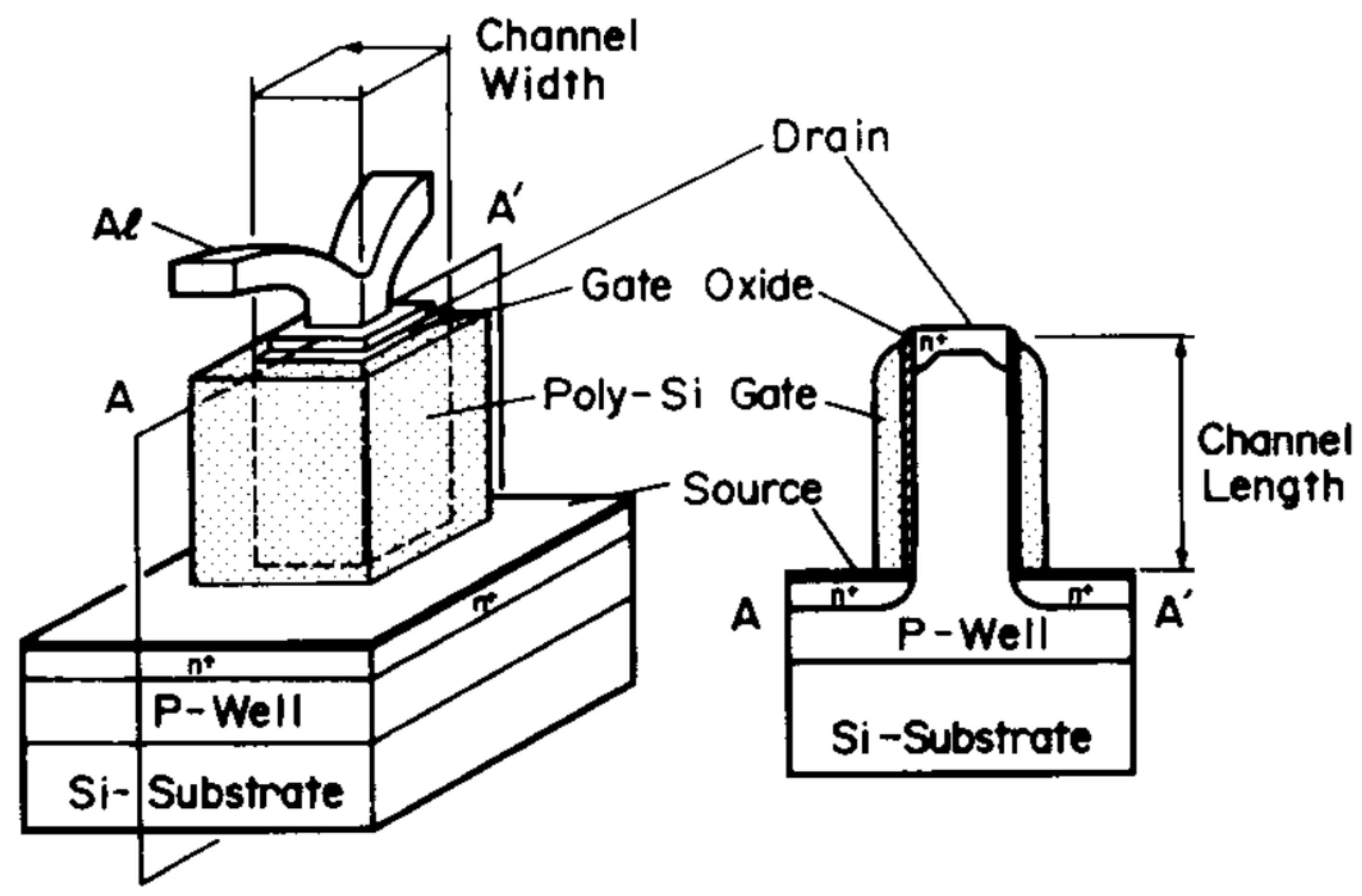
3. The vertical device in KFBM helps to improve retention and disturbance, and reduces the scaling pressure, and therefore, KBFM can provide the capability of LSI fabrication with most advanced technologies on any CMOS style process such as bulk, SOI, SGT and GAA.

4. The memory cell presented in this paper will meet the needs of a high-density embedded memory market and with specific support to expanding AI applications.

Agenda

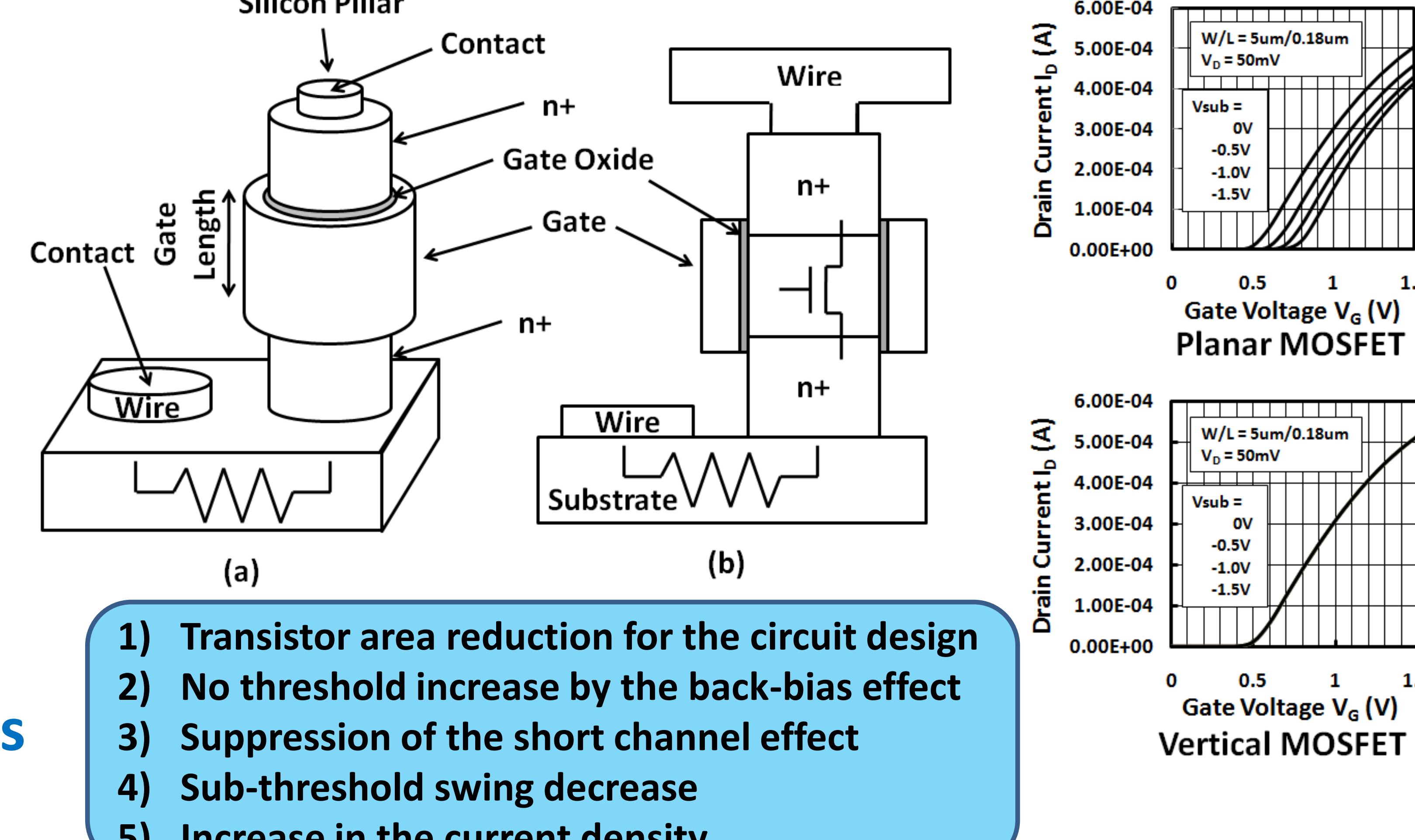
1. DFM: Dynamic Flash Memory
2. KFBM: Key shape Floating Body Memory
3. **SGT: Surrounding Gate Transistor**
4. BBCube: Bumpless Build Cube

Surrounding Gate Transistor (SGT)



1. H. Takato, K. Sunouchi, N. Okabe, A. Nitayama, K. Hieda, F. Horiguchi, and F. Masuoka, "High Performance CMOS Surrounding Gate Transistor (SGT) for Ultra High Density LSIs," in *Proc. IEDM*, pp.222-225, Dec. 1988.
2. H. Takato, K. Sunouchi, N. Okabe, A. Nitayama, K. Hieda, F. Horiguchi, and F. Masuoka, "Impact of Surrounding Gate Transistor (SGT) for Ultra-High-Density LSI' s," in *IEEE Trans. Electron Devices*, vol. 38, No. 3, pp.573-578, Mar. 1991.

SGT Structure Summary



Pros

1) Transistor area reduction for the circuit design
2) No threshold increase by the back-bias effect
3) Suppression of the short channel effect
4) Sub-threshold swing decrease
5) Increase in the current density

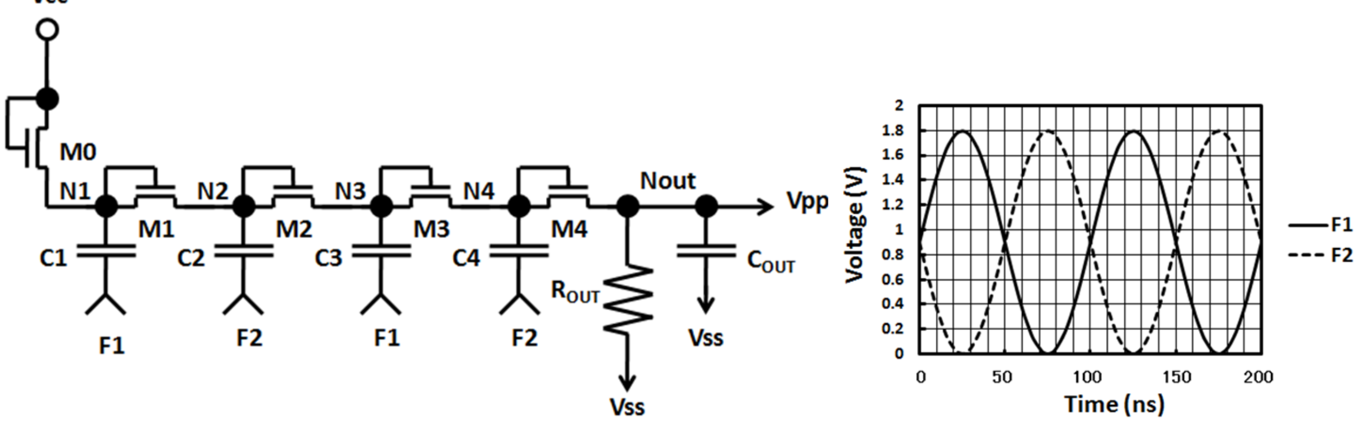
Con

1) Asymmetric source/drain transistor characteristics due to the bottom resistance

K, Sakui and T. Endoh "A Compact Space and Efficient Drain Current Design for Multipillar Vertical MOSFETs," in *IEEE Trans. Electron Devices*, vol. 57, No. 8, pp.1768-1773, Aug. 2010.

SGT Application for Charge Pump Circuit

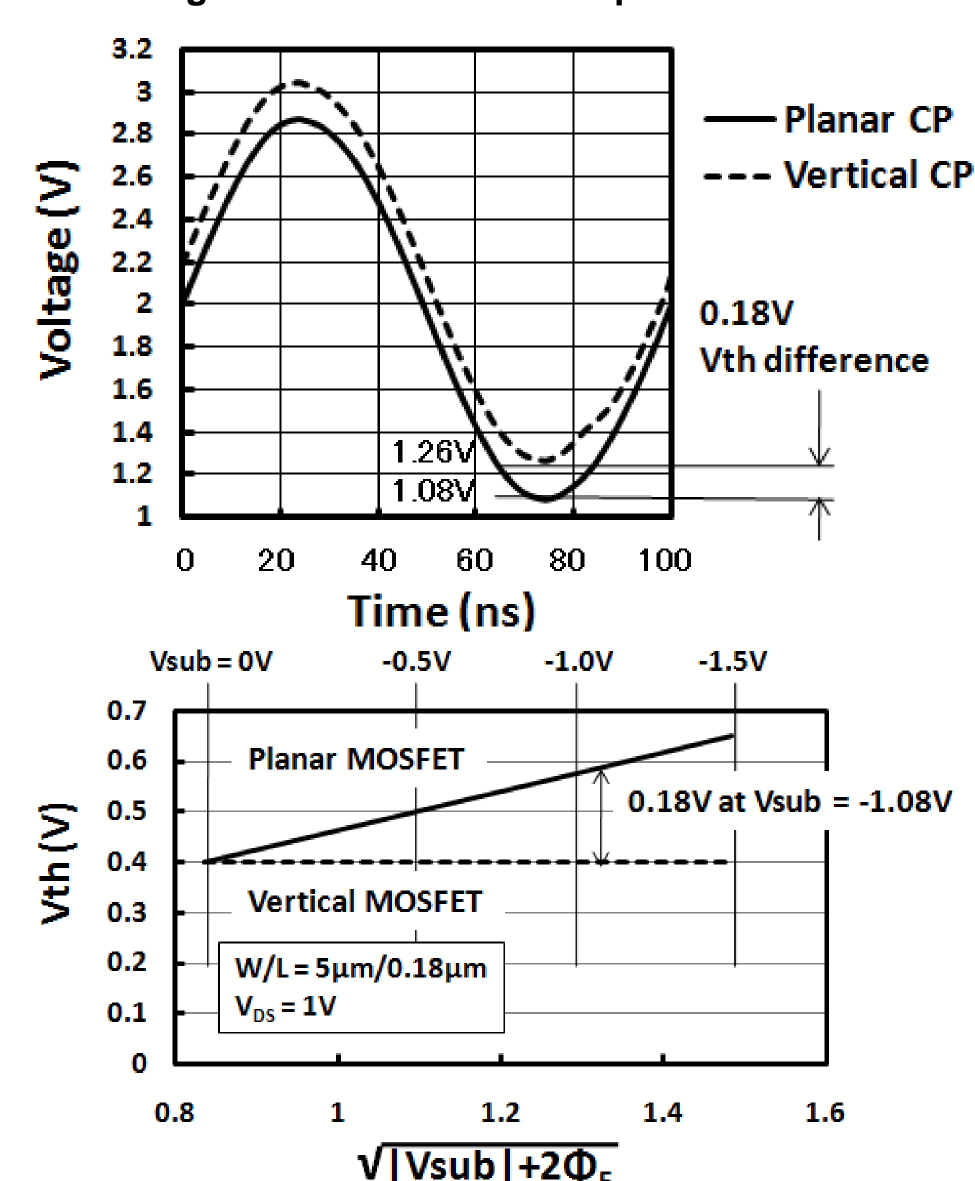
Dickson's Charge Pump Circuit



$$\Delta V = VF \times \frac{C_{1-4}}{C_{1-4} + C_S} - \frac{I_{M1-M4}}{f \times (C_{1-4} + C_S)} \quad (1)$$

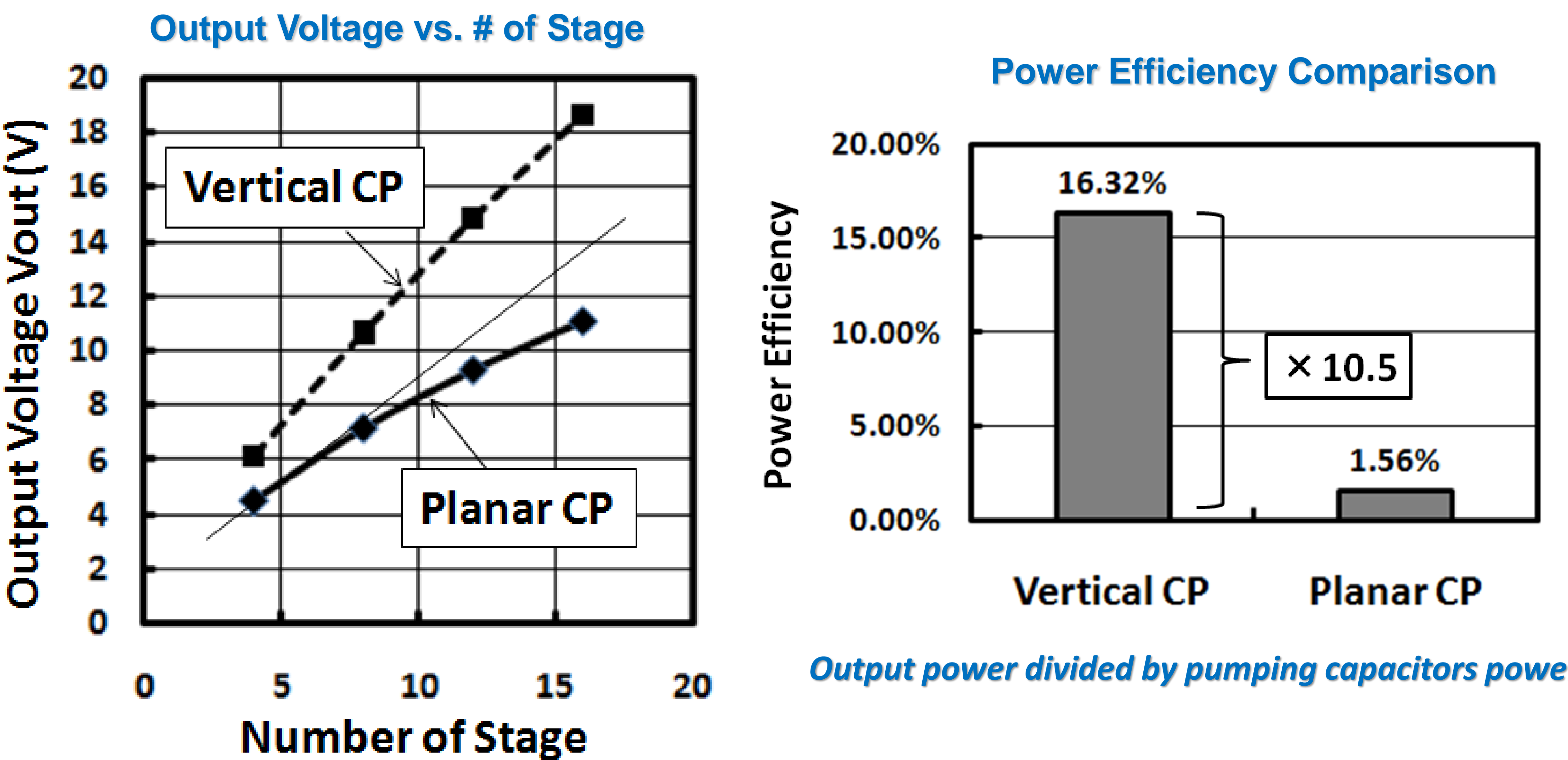
$$G_{i+1} = V_{i+1} - V_i = \Delta V - V_{th}(M_{i+1}) \quad (2)$$

First Stage Node Waveform Comparison



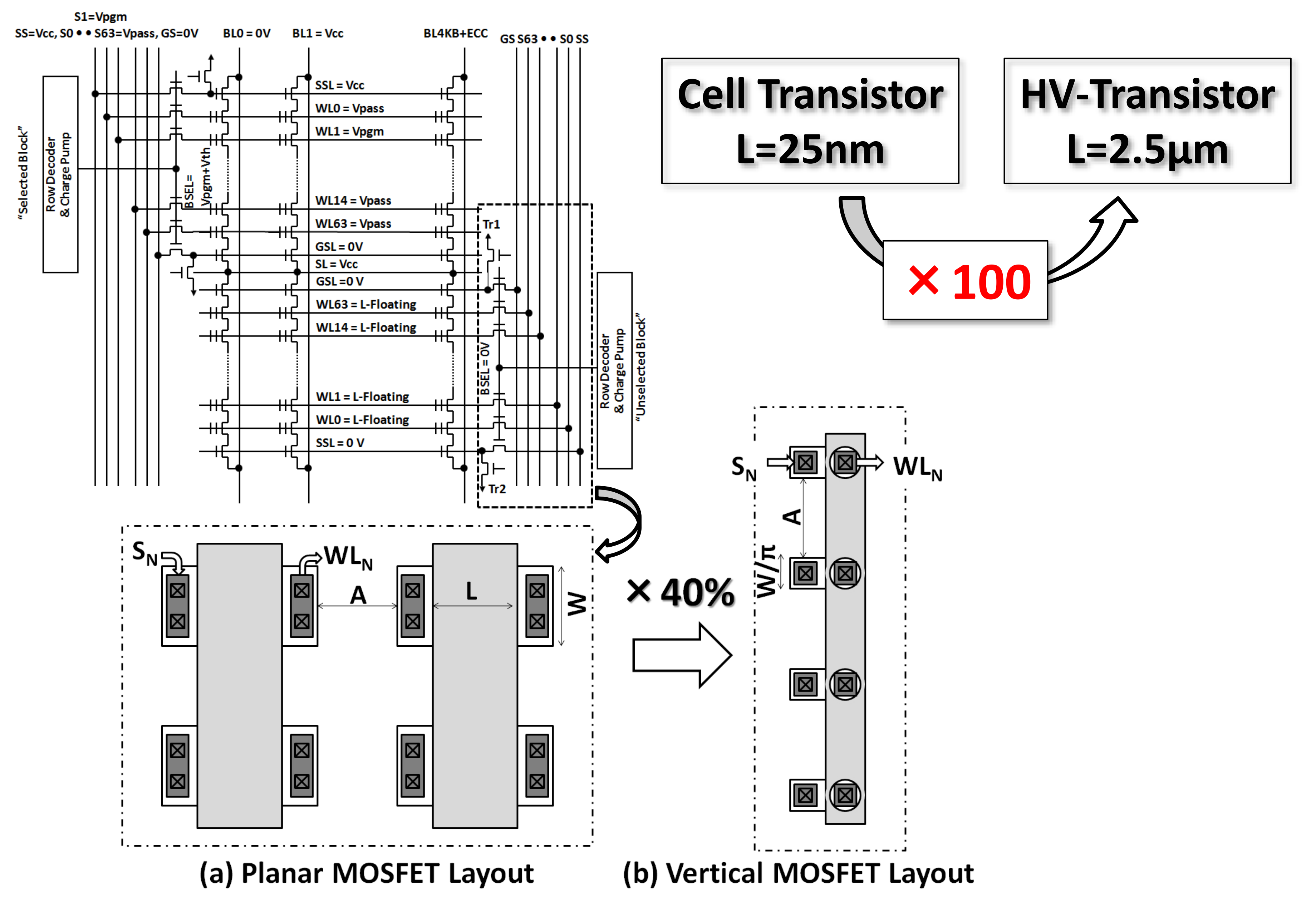
K. Sakui and T. Endoh, "Design Impacts on NAND Flash Memory Core Circuits with Vertical MOSFETs," in *Proc. IMW*, pp.84-87, May 2010.

Vertical and Planar CP's Comparison



K. Sakui and T. Endoh, "Design Impacts on NAND Flash Memory Core Circuits with Vertical MOSFETs," in *Proc. IMW*, pp.84-87, May 2010.

Row Decoder with High Voltage Transistors



(a) Planar MOSFET Layout (b) Vertical MOSFET Layout

K. Sakui and T. Endoh, "Design Impacts on NAND Flash Memory Core Circuits with Vertical MOSFETs," in *Proc. IMW*, pp.84-87, May 2010.

Cell Access Device Evolution

A. Spessot and H. Oh "1T-1C Dynamic Random Access Memory Status, Challenges, and Prospects," in *IEEE Trans. Electron Devices*, vol. 67, No. 4, pp.1382-1393, Apr. 2020.

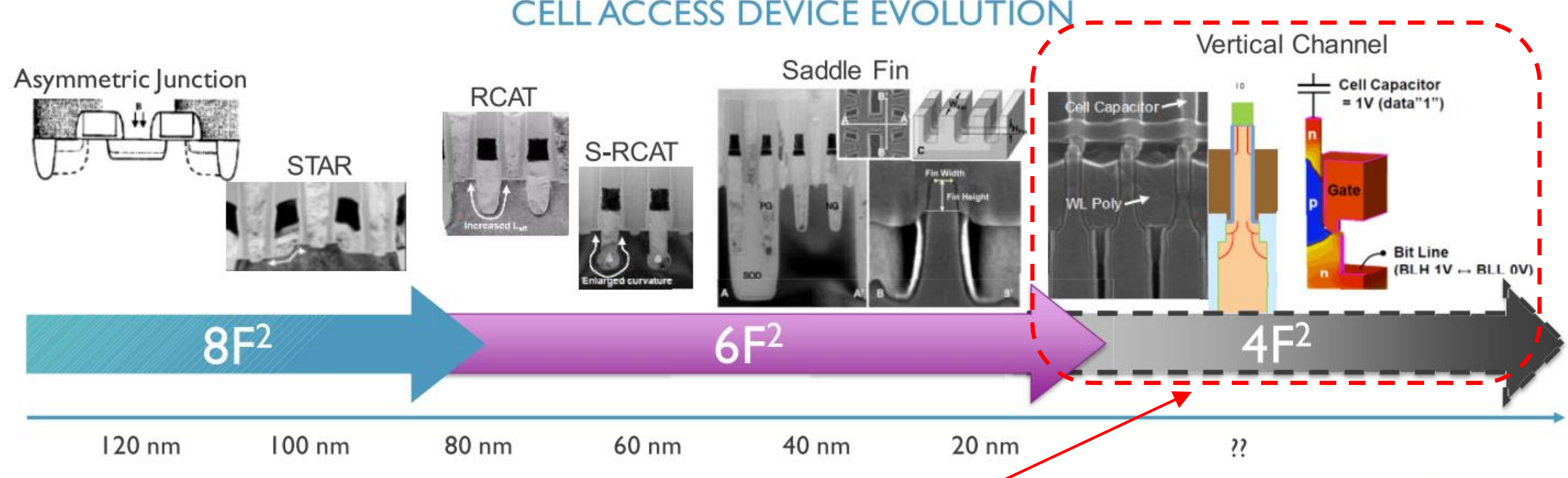
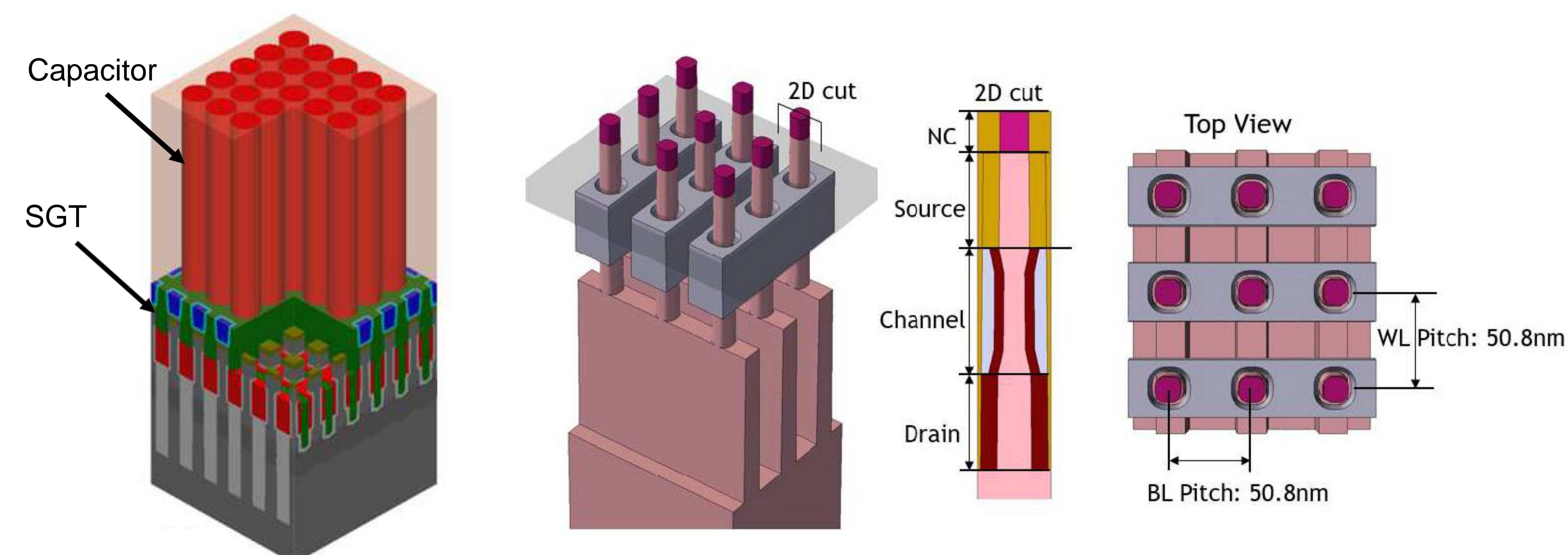


Fig. 6. Review of the historical evolution trend for the cell access device. Various cell access device options are shown. The $4F^2$ is enabled by the vertical channel. Corresponding technology nodes are included. Adapted from [5], [9], [15]–[18], [20], [22], and [23].

H. Chung et al., "Novel $4F^2$ DRAM Cell with Vertical Pillar Transistor(VPT)," 2011 Proceedings of the European Solid-State Device Research Conference (ESSDERC), pp. 211-214, Sept. 2011.

Transistor for Future $4F^2$



3D VCT (Vertical Channel Transistor) DRAM

VCT Array Access Transistor Structure

D. Feng et al., "Transistor for Future $4F^2$," in *Proc. IMW*, pp.33-36, May 2023.

Surrounding Gate Transistor With Epitaxially Grown Si Pillar

TABLE I
COMPARISON OF SADDLE FINFET AND CONVENTIONAL AND PROPOSED SGT

	Saddle FinFET	Previous SGT	SGT in this work
Layout WL, BL, SN, Silicon body, n^+ bridge	3F × 2F	2F × 2F	3F × 2F
Unit Cell Size	6F2	4F2	6F2
Channel formation	Etched silicon	Etched silicon	Epitaxial silicon
BL material	Metal	Buried n^+	Metal
Body isolation	Tied	Isolated	Isolated
Sensitive volume	Large	Small	Small

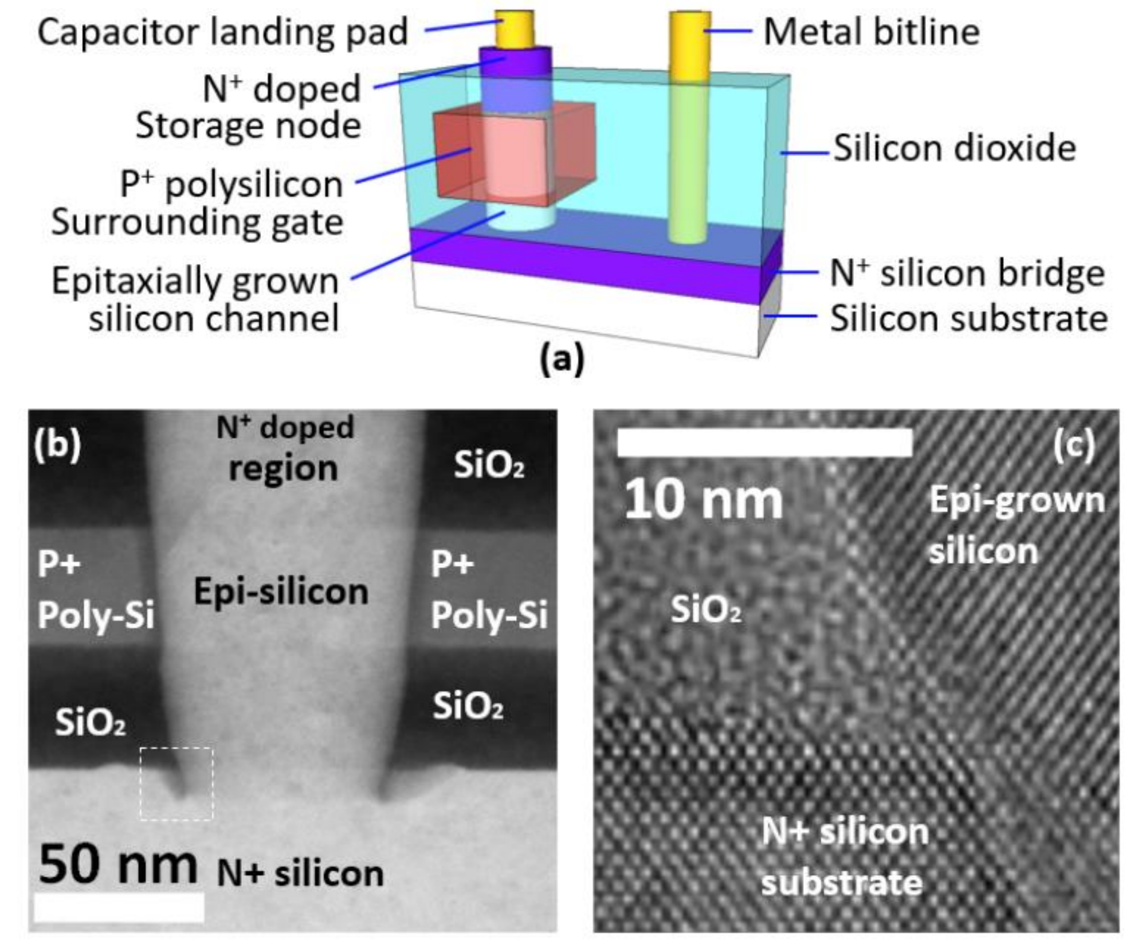


Fig. 2. (a) Schematic illustration of the final structure, (b) cross-sectional TEM image of the fabricated SGT, and (c) magnified view of the boxed region of (b).

Jin-Woo Han et al., "Surround Gate Transistor With Epitaxially Grown Si Pillar and Simulation Study on Soft Error and Row hammer Tolerance for DRAM," in *IEEE Trans. Electron Devices,* vol. 68, No. 2, pp.529-534, Feb. 2021.

SGT Conclusion

1. SGT can be used for the core circuit of the memory devices, such as the word line driver and charge pump circuit in the NAND Flash Memory, by utilizing its advantage of the back-bias free feature.

2. SGT is a candidate for the switching transistor for the memory devices, such as the DRAM and emerging memories, for realizing the $4F^2$ cell.

Agenda

1. DFM: Dynamic Flash Memory
2. KFBM: Key shape Floating Body Memory
3. SGT: Surrounding Gate Transistor
4. **BBCube: Bumpless Build Cube**

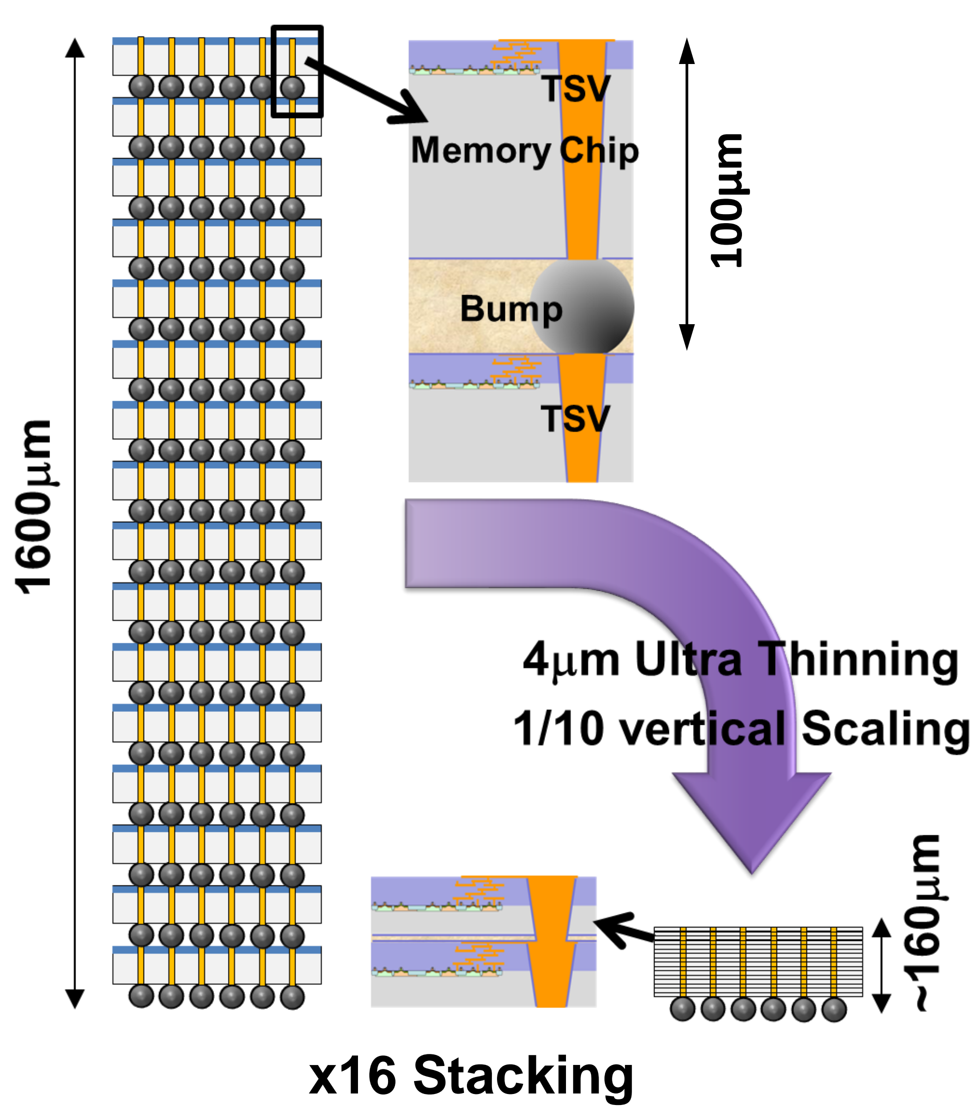
Benefits for 3D Structure with Bumpless TSV

1. Thin Die Thickness and Low Impedance

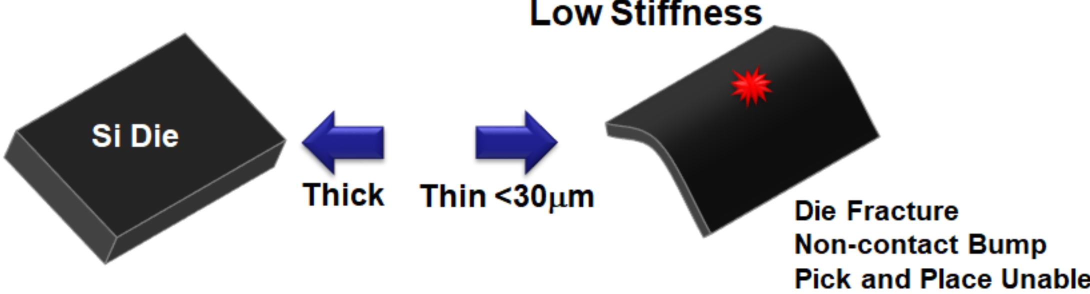
2. Massive Parallelism Availability

3. Low Heat Generation

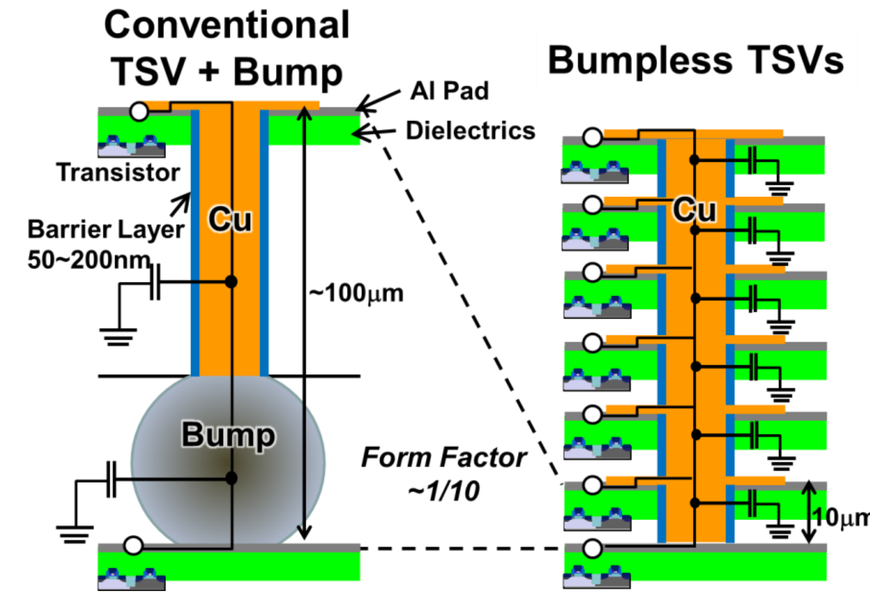
Benefit 1: Thin Die Thickness and Low Impedance



Limit of Die Thickness with Bump

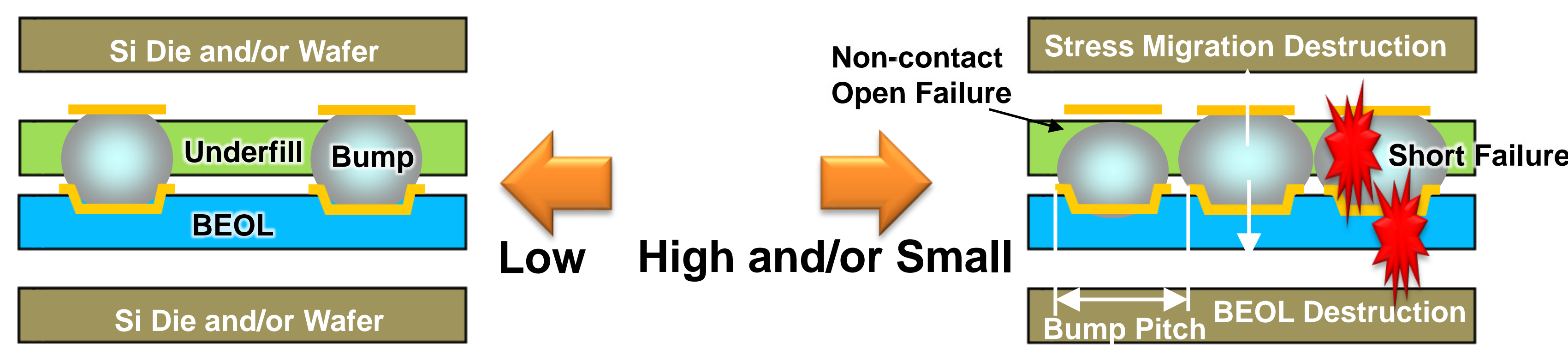


Deformation and stress occur due to CTE mismatch

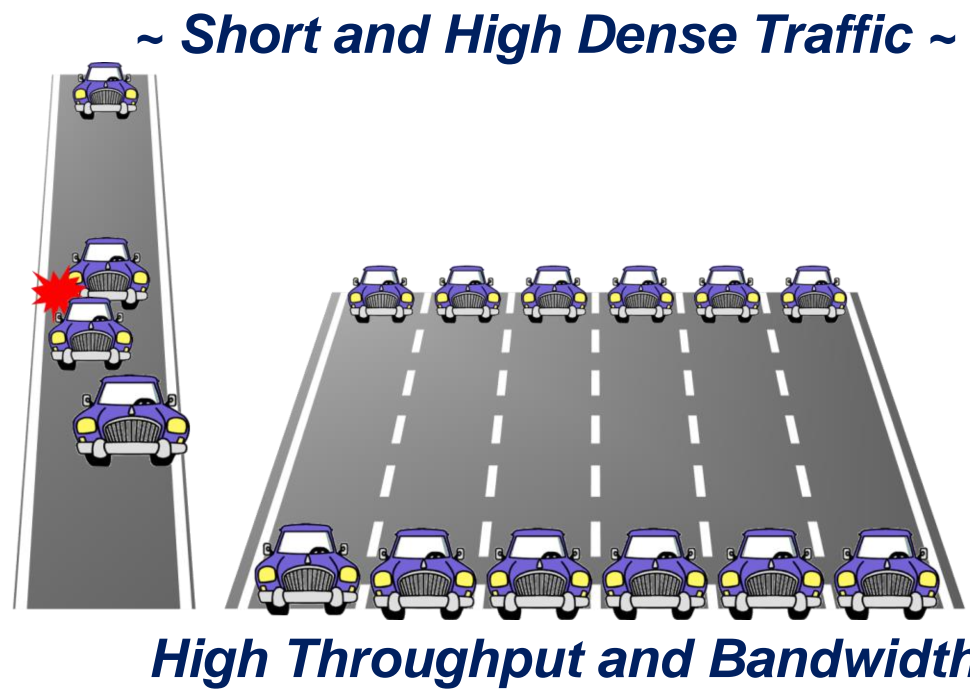


Benefit 2: Massive Parallelism Bumpless TSVs

~ Limits of Bump Size and Density ~



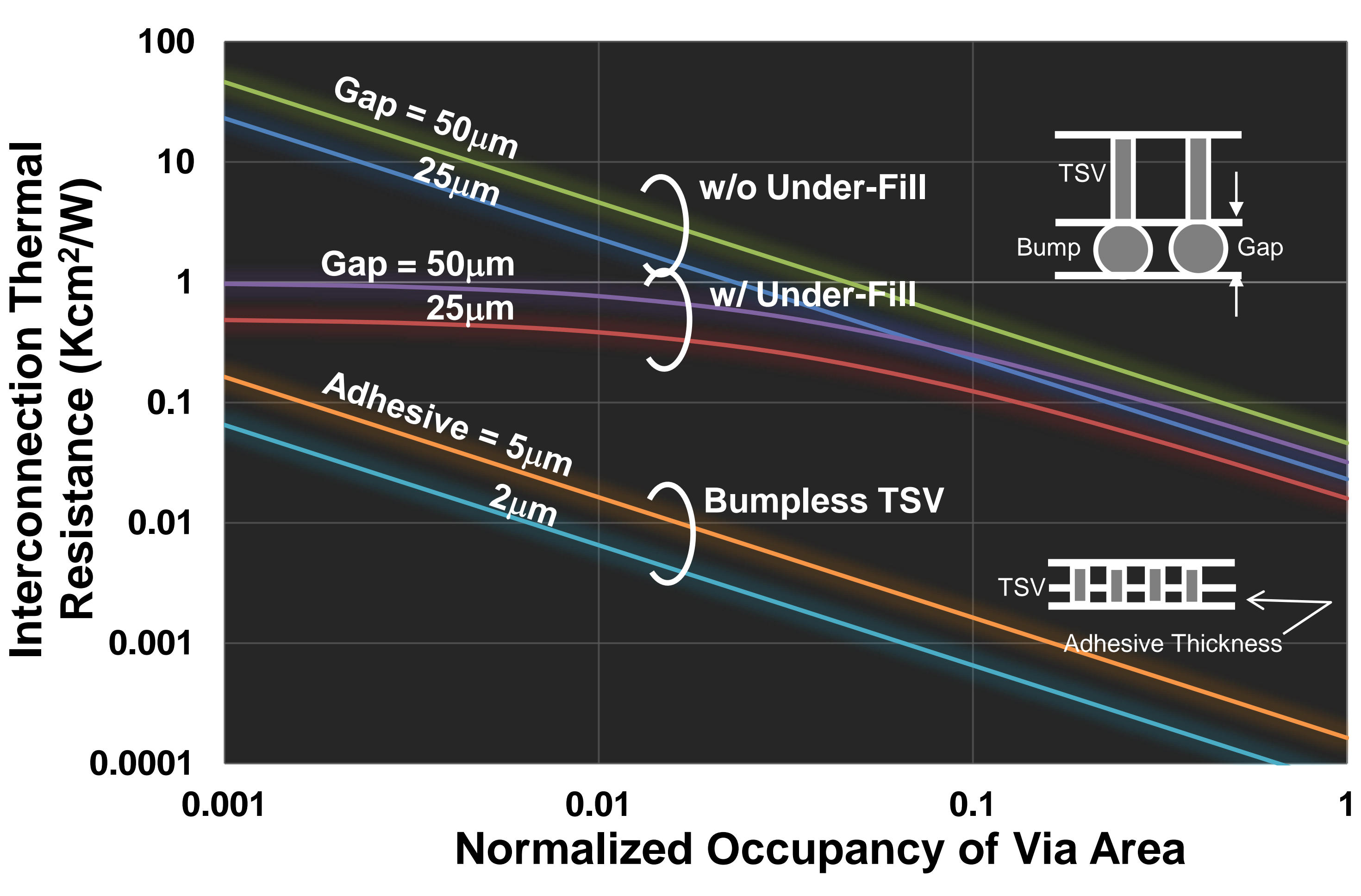
~ Short and High Dense Traffic ~



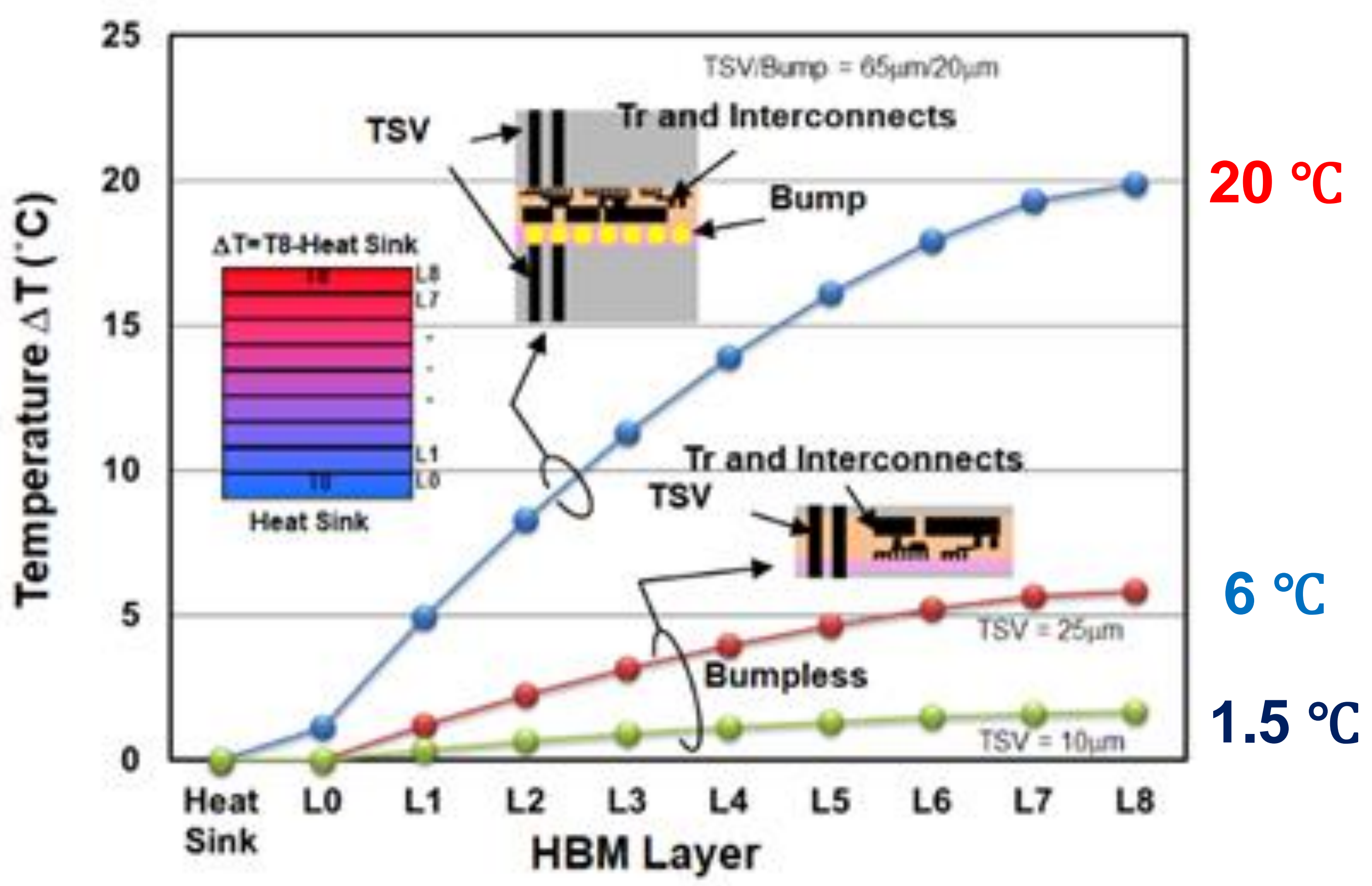
High Throughput and Bandwidth

Benefit 3: Low Heat Generation

The Bumpless Cu TSVs act like a thermal "highway."



Temperature Rise Calculation Result



20 ℃

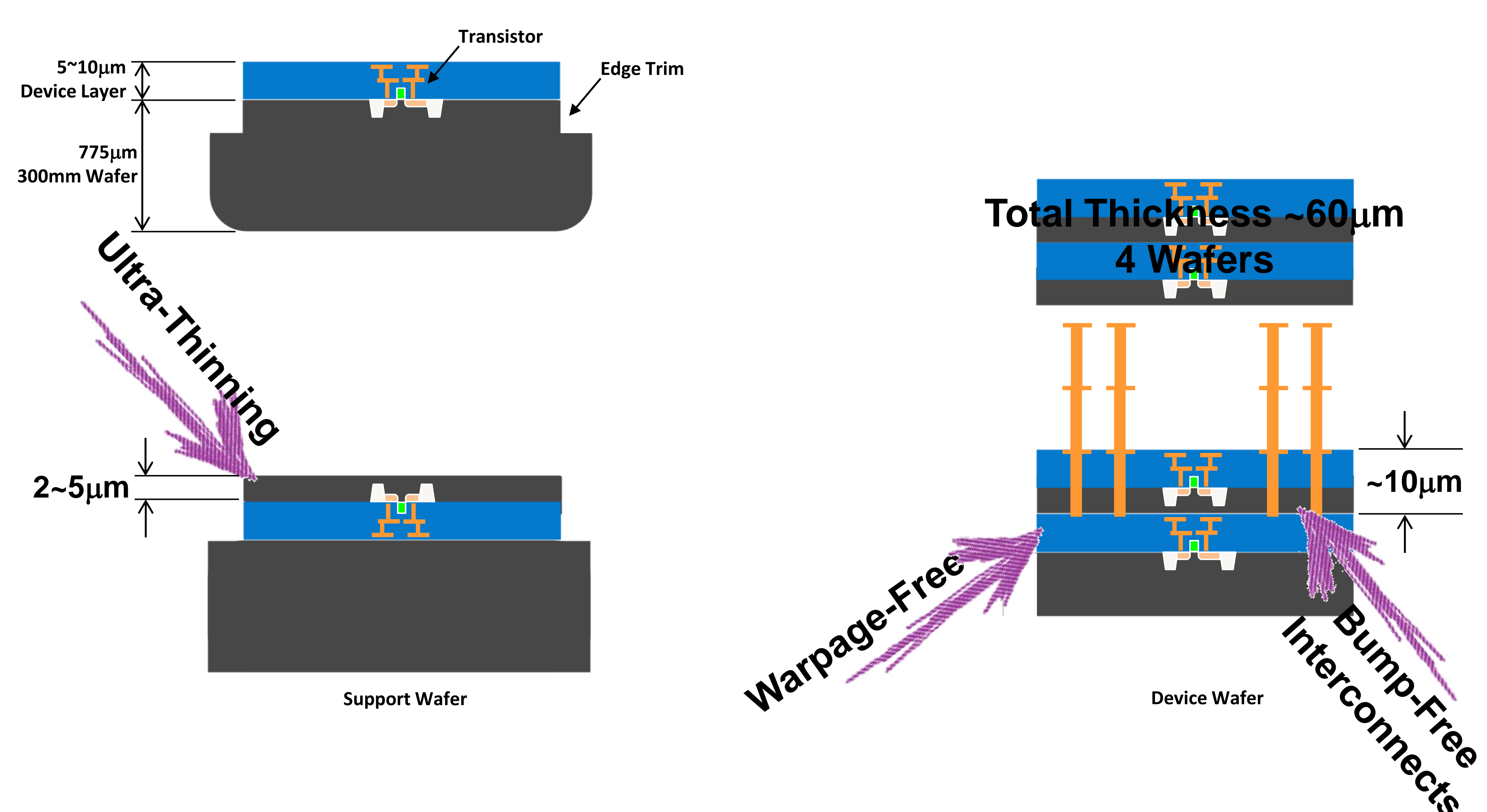
6 ℃

1.5 ℃

No refresh time modification of layer-by-layer is needed for bumpless TSV.

TSV-Last after Thinning and Bonding

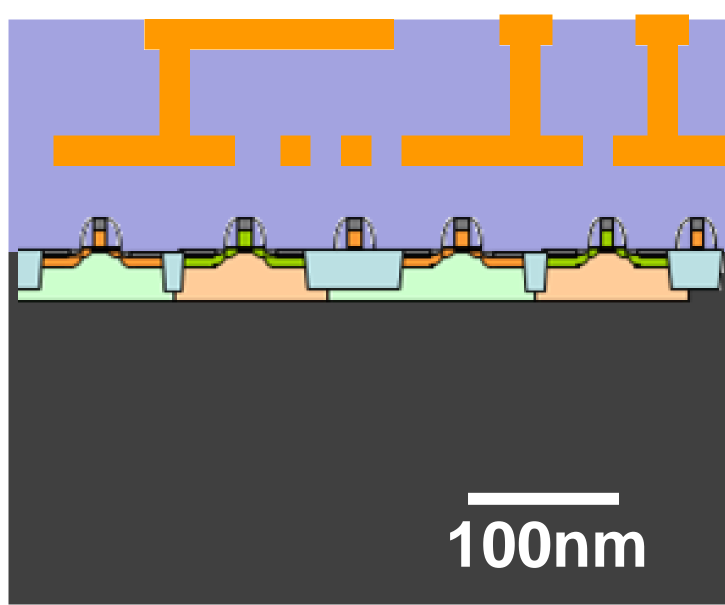
Bump-Free, Warpage-Free, and Ultra-Thin Wafer-on-Wafer Technology



Wafer Stacking and Bump-Free Process

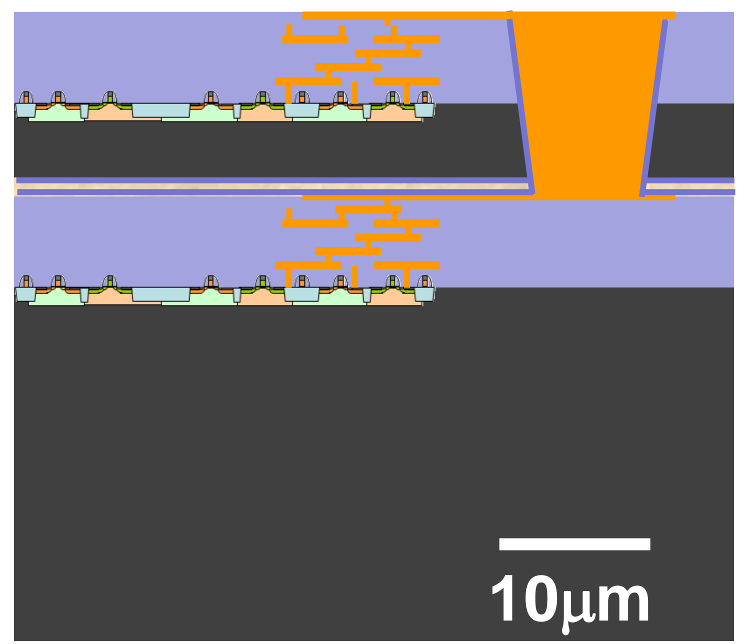
Basic idea is based on BEOL compatibility.

✓Dielectrics Deposition
✓Dual-Damascene Etching
✓Cu Plug and Metallization



(a) Cu/Low-k Interconnects

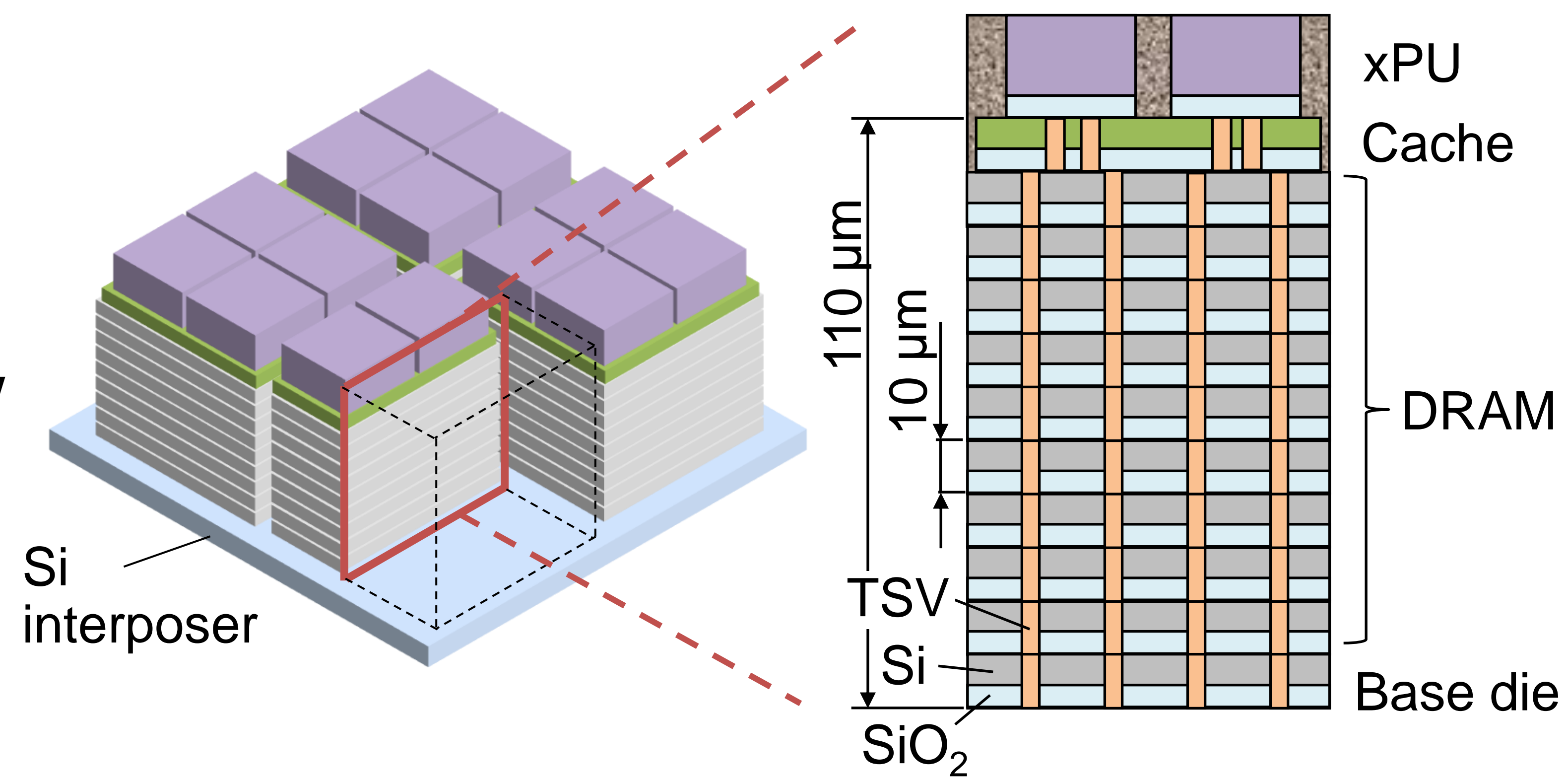
✓Thinned Wafer Bonding
✓Dual-Damascene TSV Etching
✓Cu Plug and Metallization



(b) Bump-Free TSV Interconnects

Structure of BBCube 3D

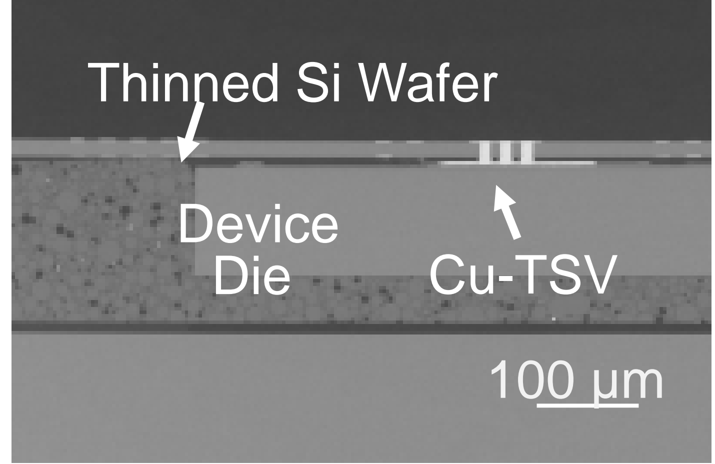
- BBCube 3D comprises
  - Multiple xPU chiplets
  - Last level cache die
  - Laminated DRAMs
  - Base die
- Stacked by WoW and CoW



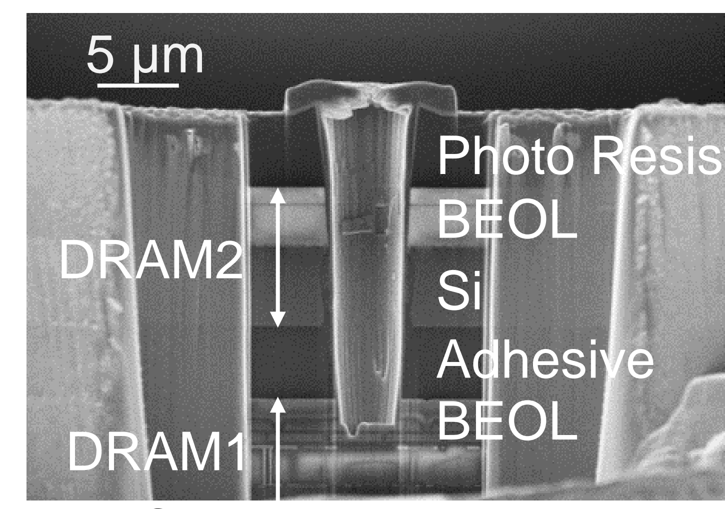
1. N. Chujo, H. Ryoson, K. Sakui, S. Sugatani, T. Nakamura, and T. Ohba, "Electrical and Thermal Analysis of Bumpless Build Cube 3D Using Wafer-on-Wafer and Chip-on-Wafer for Near Memory Computing," in *Proc. ECTC*, pp.772-777, May 2023.
2. N. Chujo, K. Sakui, S. Sugatani, H. Ryoson, T. Nakamura, and T. Ohba, "Bumpless Build Cube (BBCube) 3D: Heterogeneous 3D Integration Using WoW and CoW to Provide TB/s Bandwidth with Lowest Bit Access Energy," in *Symposium on VLSI Technology and Circuits Digest of Technical Papers*, JFS4-4, pp.1-2, Jun. 2023.

Structure of BBCube 3D

- Bumpless Via-Last interconnect similar to Cu/Low-k BEOL process
  - Stacking and thinning first, TSV formation last
  - Wafer/die bonding used SiOC adhesives. No needs nano-scale planarization
  - BEOL-based high reliability interconnects with low-thermal budget
- Ultra-thinning
  - Low TSV aspect ratio down to 2.5
  - Low cost interconnects compared to conventional 3DIs using micro-bumps and hybrid bonding



Cross-section of CoW



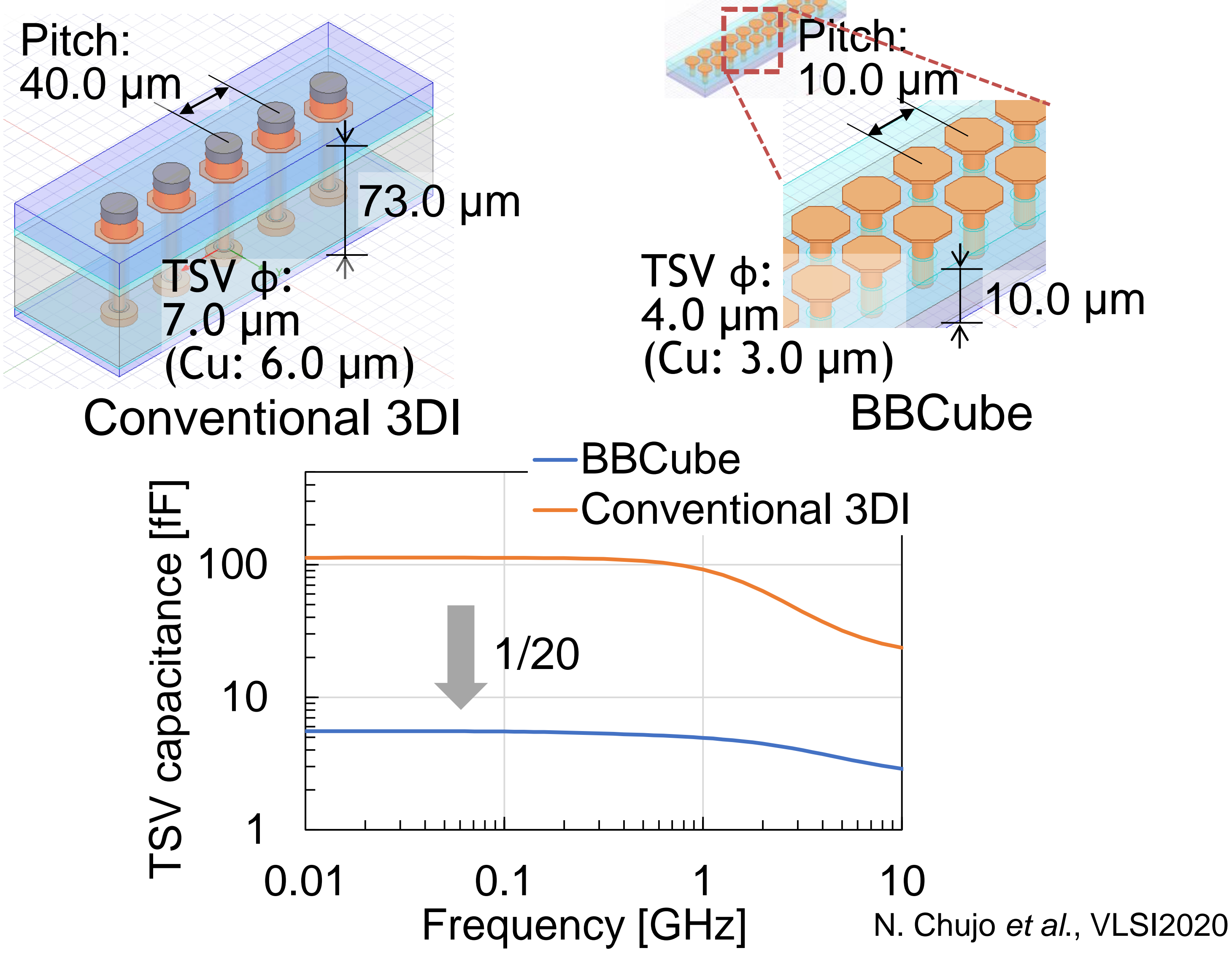
Cross-section of WoW

T. Funaki *et al.*, ECTC2021
T. Takasaki *et al.* DPS2021

1. N. Chujo, H. Ryoson, K. Sakui, S. Sugatani, T. Nakamura, and T. Ohba, "Electrical and Thermal Analysis of Bumpless Build Cube 3D Using Wafer-on-Wafer and Chip-on-Wafer for Near Memory Computing," in *Proc. ECTC*, pp.772-777, May 2023.
2. N. Chujo, K. Sakui, S. Sugatani, H. Ryoson, T. Nakamura, and T. Ohba, "Bumpless Build Cube (BBCube) 3D: Heterogeneous 3D Integration Using WoW and CoW to Provide TB/s Bandwidth with Lowest Bit Access Energy," in *Symposium on VLSI Technology and Circuits Digest of Technical Papers*, JFS4-4, pp.1-2, Jun. 2023.

Superior Connectivity of BBCube

- BBCube features
  - High-density TSVs
  - Low-capacitance TSVs
- Towards low power consumption
  - High parallelism
    → Low data rate
  - 3D placement
    → Low capacitance

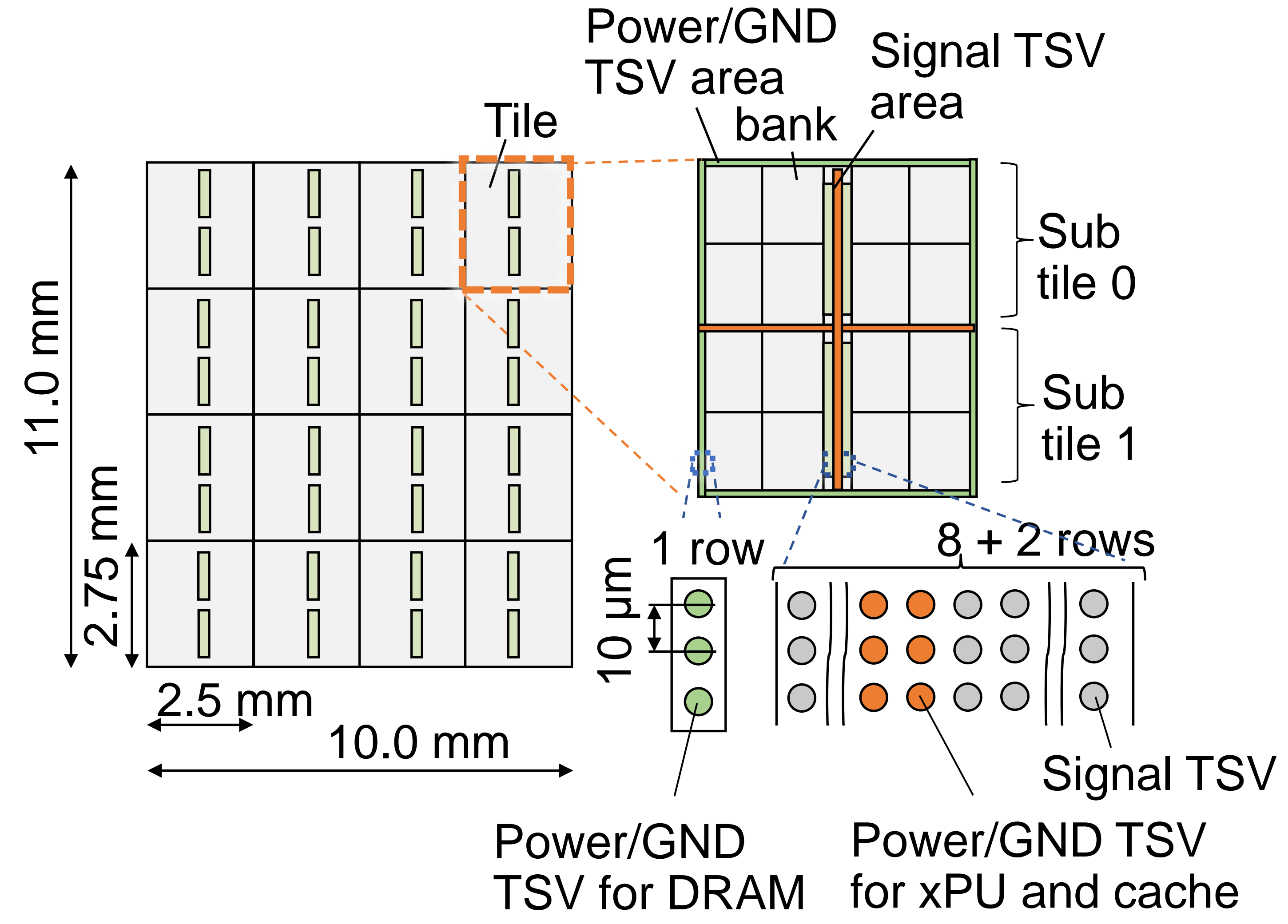


N. Chujo *et al.*, VLSI2020

1. N. Chujo, H. Ryoson, K. Sakui, S. Sugatani, T. Nakamura, and T. Ohba, "Electrical and Thermal Analysis of Bumpless Build Cube 3D Using Wafer-on-Wafer and Chip-on-Wafer for Near Memory Computing," in *Proc. ECTC*, pp.772-777, May 2023.
2. N. Chujo, K. Sakui, S. Sugatani, H. Ryoson, T. Nakamura, and T. Ohba, "Bumpless Build Cube (BBCube) 3D: Heterogeneous 3D Integration Using WoW and CoW to Provide TB/s Bandwidth with Lowest Bit Access Energy," in *Symposium on VLSI Technology and Circuits Digest of Technical Papers*, JFS4-4, pp.1-2, Jun. 2023.

DRAM Design Assumed for BBCube

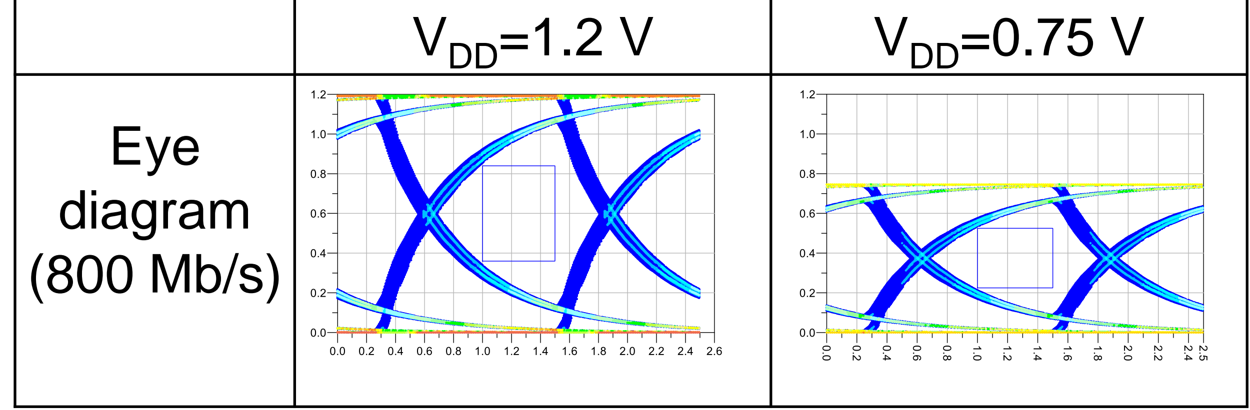
- High parallelism design
  - 16K I/Os
  - 16 tiles in a die
  - 1024 I/Os in each tile
- Data rate is set at 800 Mb/s BW reaches 1.6 TB/s
  - 1/4X data rate of HBM2E
  - 4X higher BW than HBM2E

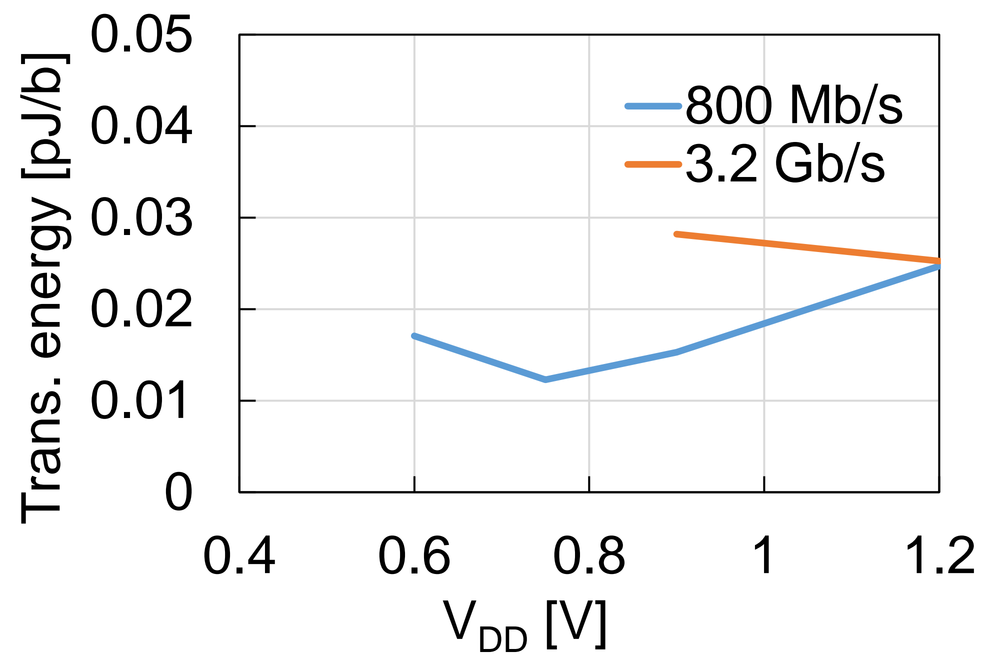


1. N. Chujo, H. Ryoson, K. Sakui, S. Sugatani, T. Nakamura, and T. Ohba, "Electrical and Thermal Analysis of Bumpless Build Cube 3D Using Wafer-on-Wafer and Chip-on-Wafer for Near Memory Computing," in *Proc. ECTC*, pp.772-777, May 2023.
2. N. Chujo, K. Sakui, S. Sugatani, H. Ryoson, T. Nakamura, and T. Ohba, "Bumpless Build Cube (BBCube) 3D: Heterogeneous 3D Integration Using WoW and CoW to Provide TB/s Bandwidth with Lowest Bit Access Energy," in *Symposium on VLSI Technology and Circuits Digest of Technical Papers*, JFS4-4, pp.1-2, Jun. 2023.

I/O Power Supply Voltage

- 1/4X data rate
  - Power supply voltage can be lowered to 0.75 V
  - TSV transmission energy can be reduced to 1/60X that of HBM2E

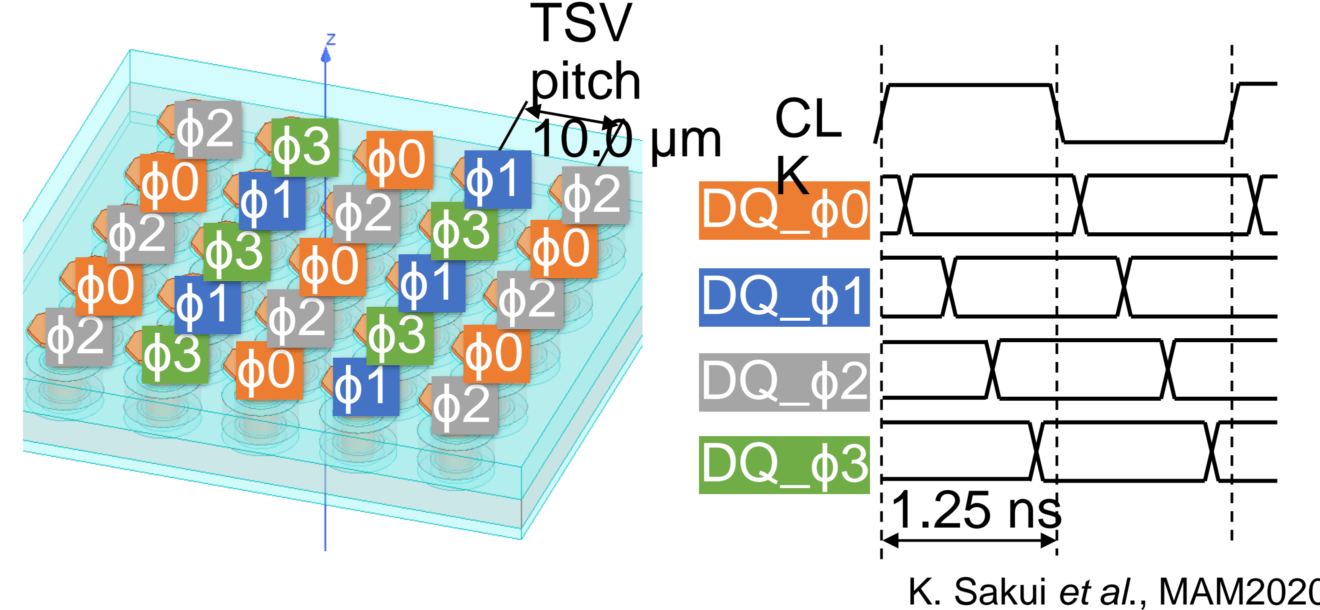




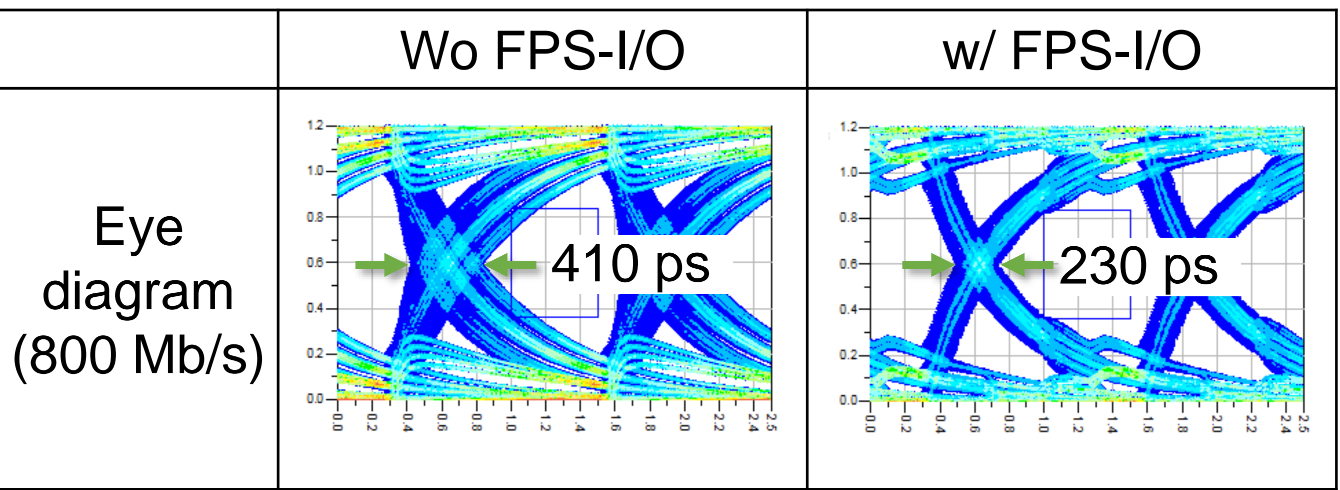
1. N. Chujo, H. Ryoson, K. Sakui, S. Sugatani, T. Nakamura, and T. Ohba, "Electrical and Thermal Analysis of Bumpless Build Cube 3D Using Wafer-on-Wafer and Chip-on-Wafer for Near Memory Computing," in *Proc. ECTC*, pp.772-777, May 2023.
2. N. Chujo, K. Sakui, S. Sugatani, H. Ryoson, T. Nakamura, and T. Ohba, "Bumpless Build Cube (BBCube) 3D: Heterogeneous 3D Integration Using WoW and CoW to Provide TB/s Bandwidth with Lowest Bit Access Energy," in *Symposium on VLSI Technology and Circuits Digest of Technical Papers*, JFS4-4, pp.1-2, Jun. 2023.

Four-phase Shielded I/O

- To reduce crosstalk noise
  - All adjacent I/Os are set to be out of phase in 90° steps
  - At a cross point of an I/O, surrounding I/Os are in a stable state



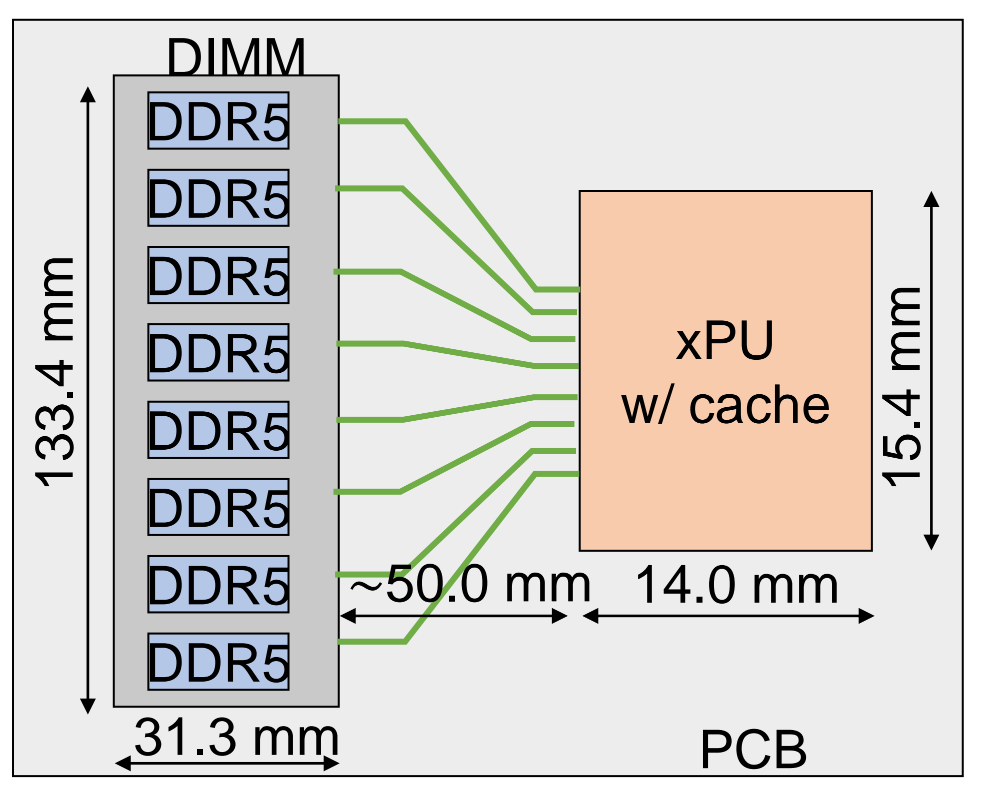
K. Sakui *et al.*, MAM2020



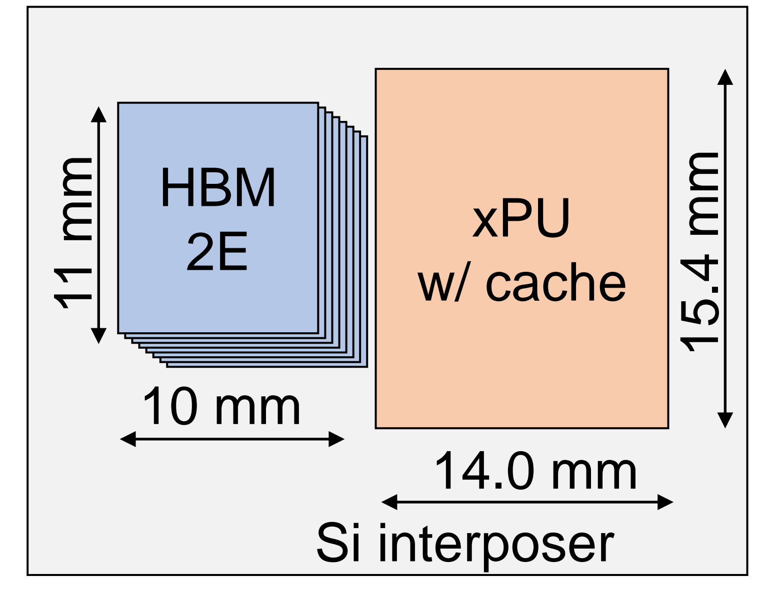
1. N. Chujo, H. Ryoson, K. Sakui, S. Sugatani, T. Nakamura, and T. Ohba, "Electrical and Thermal Analysis of Bumpless Build Cube 3D Using Wafer-on-Wafer and Chip-on-Wafer for Near Memory Computing," in *Proc. ECTC*, pp.772-777, May 2023.
2. N. Chujo, K. Sakui, S. Sugatani, H. Ryoson, T. Nakamura, and T. Ohba, "Bumpless Build Cube (BBCube) 3D: Heterogeneous 3D Integration Using WoW and CoW to Provide TB/s Bandwidth with Lowest Bit Access Energy," in *Symposium on VLSI Technology and Circuits Digest of Technical Papers*, JFS4-4, pp.1-2, Jun. 2023.

Size and Arrangement

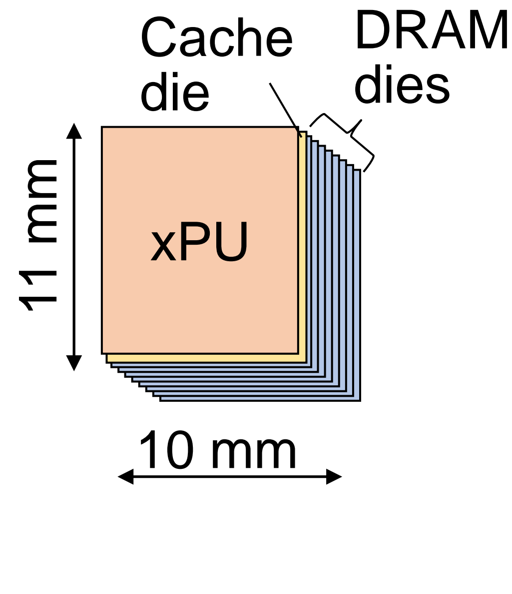
- DDR5 and HBM: xPU includes cache in a die
- BBCube: xPU core and cache are on different dies



DDR5



HBM2E

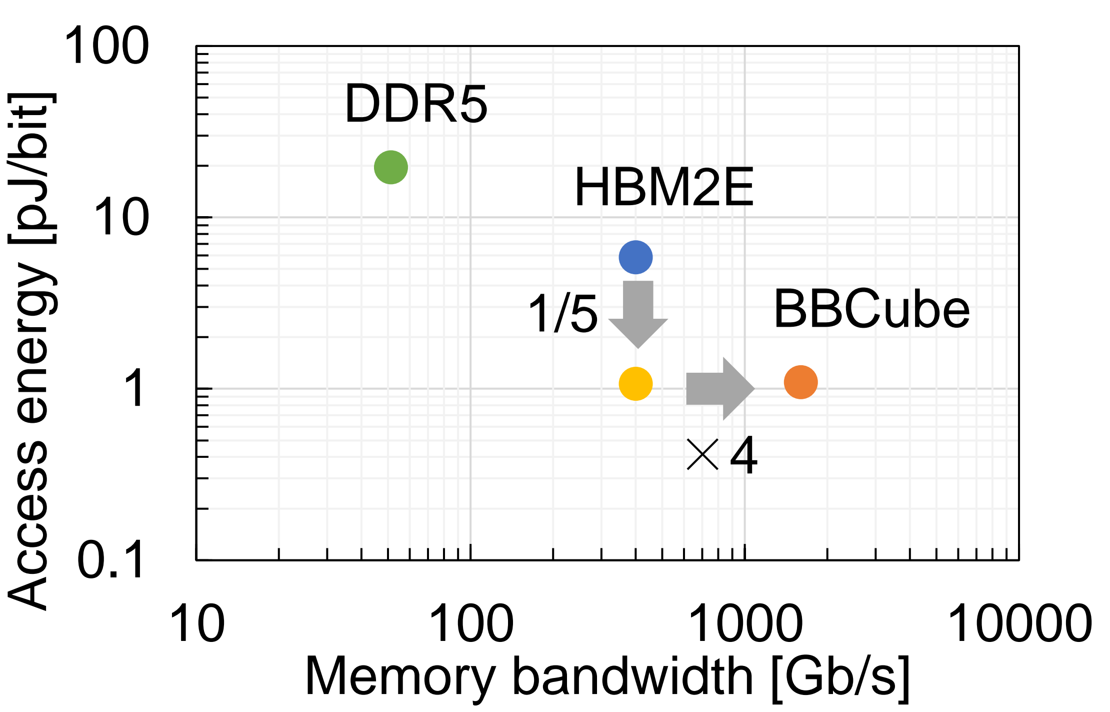


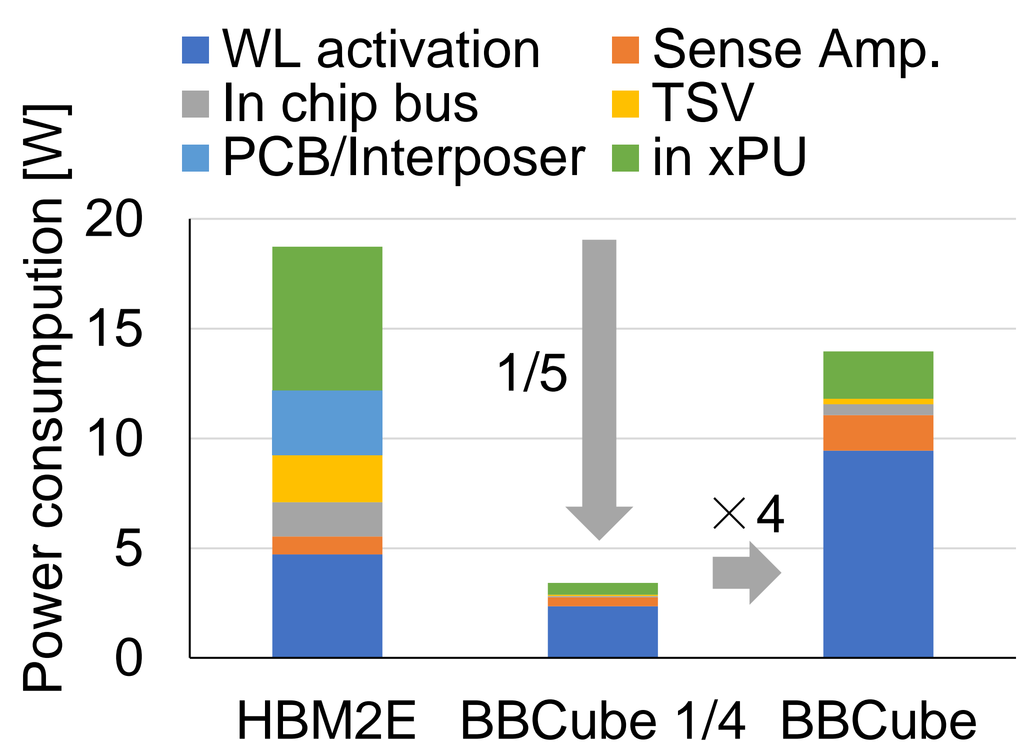
BBCube

1. N. Chujo, H. Ryoson, K. Sakui, S. Sugatani, T. Nakamura, and T. Ohba, "Electrical and Thermal Analysis of Bumpless Build Cube 3D Using Wafer-on-Wafer and Chip-on-Wafer for Near Memory Computing," in *Proc. ECTC*, pp.772-777, May 2023.
2. N. Chujo, K. Sakui, S. Sugatani, H. Ryoson, T. Nakamura, and T. Ohba, "Bumpless Build Cube (BBCube) 3D: Heterogeneous 3D Integration Using WoW and CoW to Provide TB/s Bandwidth with Lowest Bit Access Energy," in *Symposium on VLSI Technology and Circuits Digest of Technical Papers*, JFS4-4, pp.1-2, Jun. 2023.

Bit Access Energy Comparison

- BBCube 3D reaches
  - 30X higher bandwidth, 20X lower access energy than DDR5
  - 4X higher bandwidth, 5X lower access energy than HBM2E





1. N. Chujo, H. Ryoson, K. Sakui, S. Sugatani, T. Nakamura, and T. Ohba, "Electrical and Thermal Analysis of Bumpless Build Cube 3D Using Wafer-on-Wafer and Chip-on-Wafer for Near Memory Computing," in *Proc. ECTC*, pp.772-777, May 2023.
2. N. Chujo, K. Sakui, S. Sugatani, H. Ryoson, T. Nakamura, and T. Ohba, "Bumpless Build Cube (BBCube) 3D: Heterogeneous 3D Integration Using WoW and CoW to Provide TB/s Bandwidth with Lowest Bit Access Energy," in *Symposium on VLSI Technology and Circuits Digest of Technical Papers*, JFS4-4, pp.1-2, Jun. 2023.

Perceptional Change From 2D to 3D ⇒ From Line Access to Plane Access

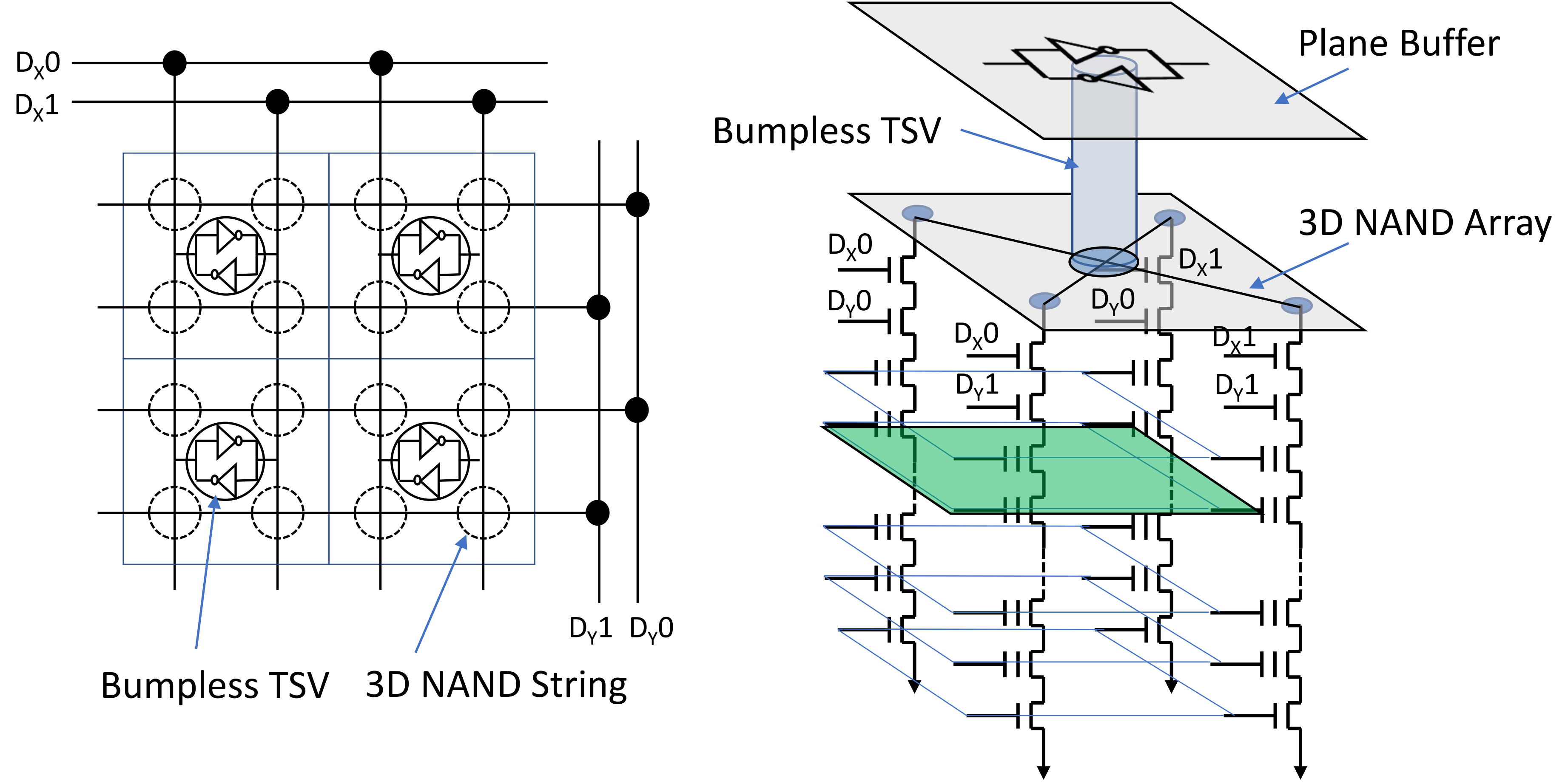
For speed up of memory access, Parallelism should be enhanced!

- **Word Line** ⇒ **Word Plate**
- **Horizontal Bit Line** ⇒ **Vertical Bit Line**
- **Page Buffer** ⇒ **Plane Buffer**

1. K. Sakui and T. Ohba, "High Speed, Low Power, and Ultra-small Operating Platform with Three-dimensional Integration (3DI) by Bumpless interconnects," in the *IEEE IMW Dig. Tech. Papers*, pp.60-63, May 2019. .
2. K. Sakui and T. Ohba, "High Bandwidth Memory (HBM) and High Bandwidth NAND (HBN) with the Bumpless TSV Technology," in the *IEEE 2019 International 3D Systems Integration Conference Dig. Tech. Papers*, Paper Id: 3DIC2019.4005, Oct 2019.
3. T. Ohba, K. Sakui, S. Sugatani, H. Ryoson, and N. Chujo, "Review of Bumpless Build Cube (BBCube) Using Wafer-o n-Wafer (WOW) and Chip-on-Wafer (COW) for Tera-Scale Three-Dimensional Integration (3DI)," *Electronics 2022*, 11(2), doi:10.3390/electronics11020236, pp.1-52, 2022.

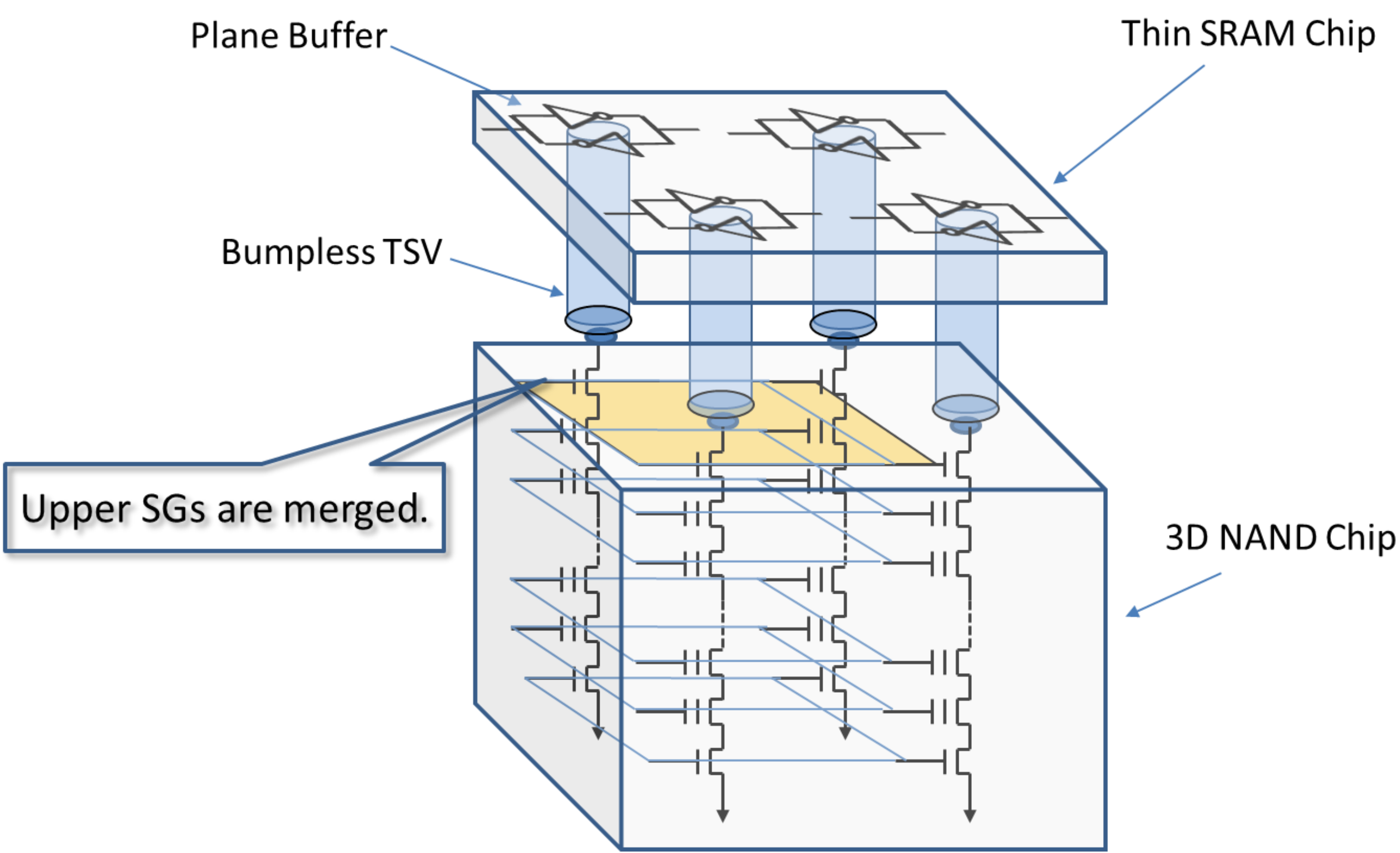
Example: High Bandwidth NAND (HBN), 3D DRAM is similar

Word Line Access ⇒ Word Plate Access



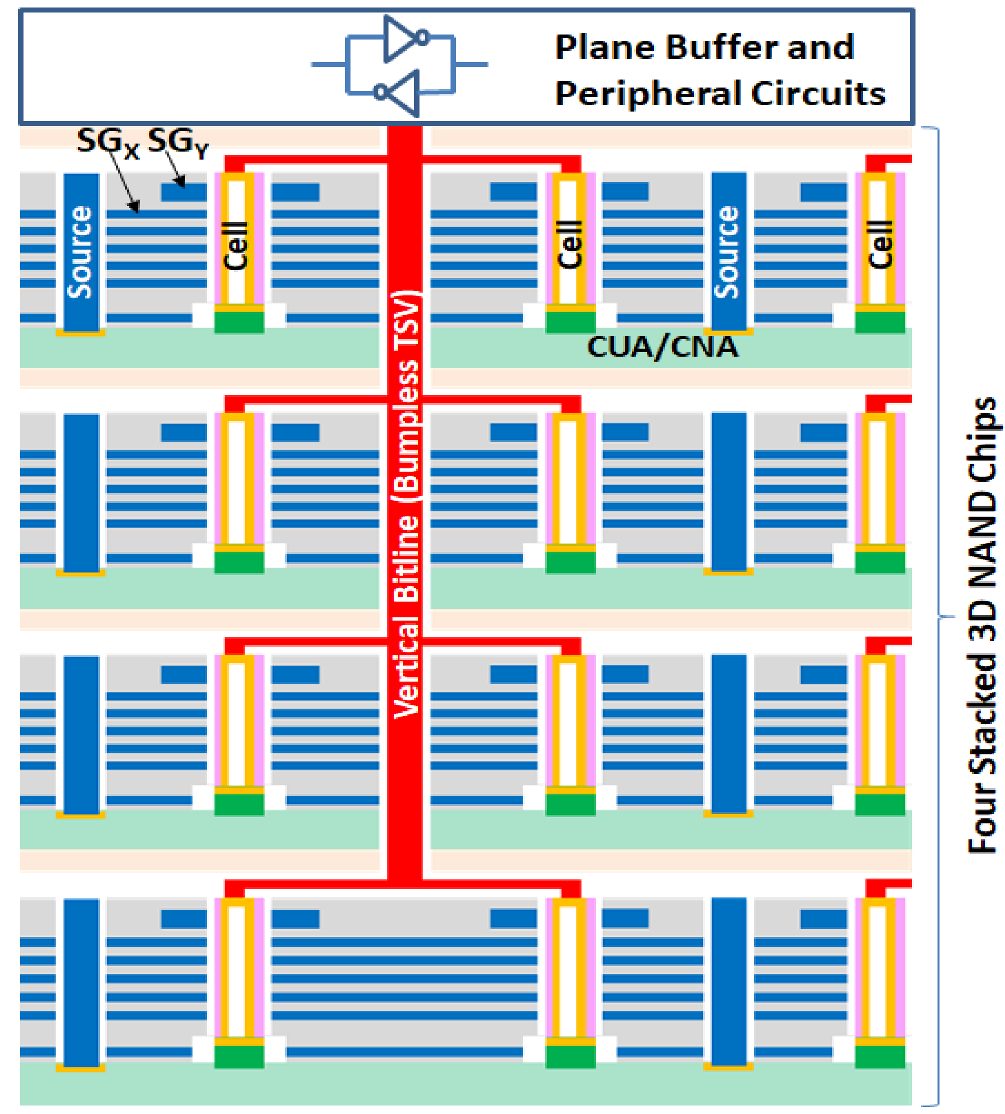
1. K. Sakui and T. Ohba, “High Speed, Low Power, and Ultra-small Operating Platform with Three-dimensional Integration (3DI) by Bumpless interconnects,” in the *IEEE IMW Dig. Tech. Papers*, pp.60-63, May 2019. .
2. K. Sakui and T. Ohba, “High Bandwidth Memory (HBM) and High Bandwidth NAND (HBN) with the Bumpless TSV Technology,” in the *IEEE 2019 International 3D Systems Integration Conference Dig. Tech. Papers*, Paper Id: 3DIC2019.4005, Oct 2019.
3. T. Ohba, K. Sakui, S. Sugatani, H. Ryoson, and N. Chujo, “Review of Bumpless Build Cube (BBCube) Using Wafer-o n-Wafer (WOW) and Chip-on-Wafer (COW) for Tera-Scale Three-Dimensional Integration (3DI),” *Electronics 2022*, 11(2), doi:10.3390/electronics11020236, pp.1-52, 2022.

Ultimate Structure for High Bandwidth NAND



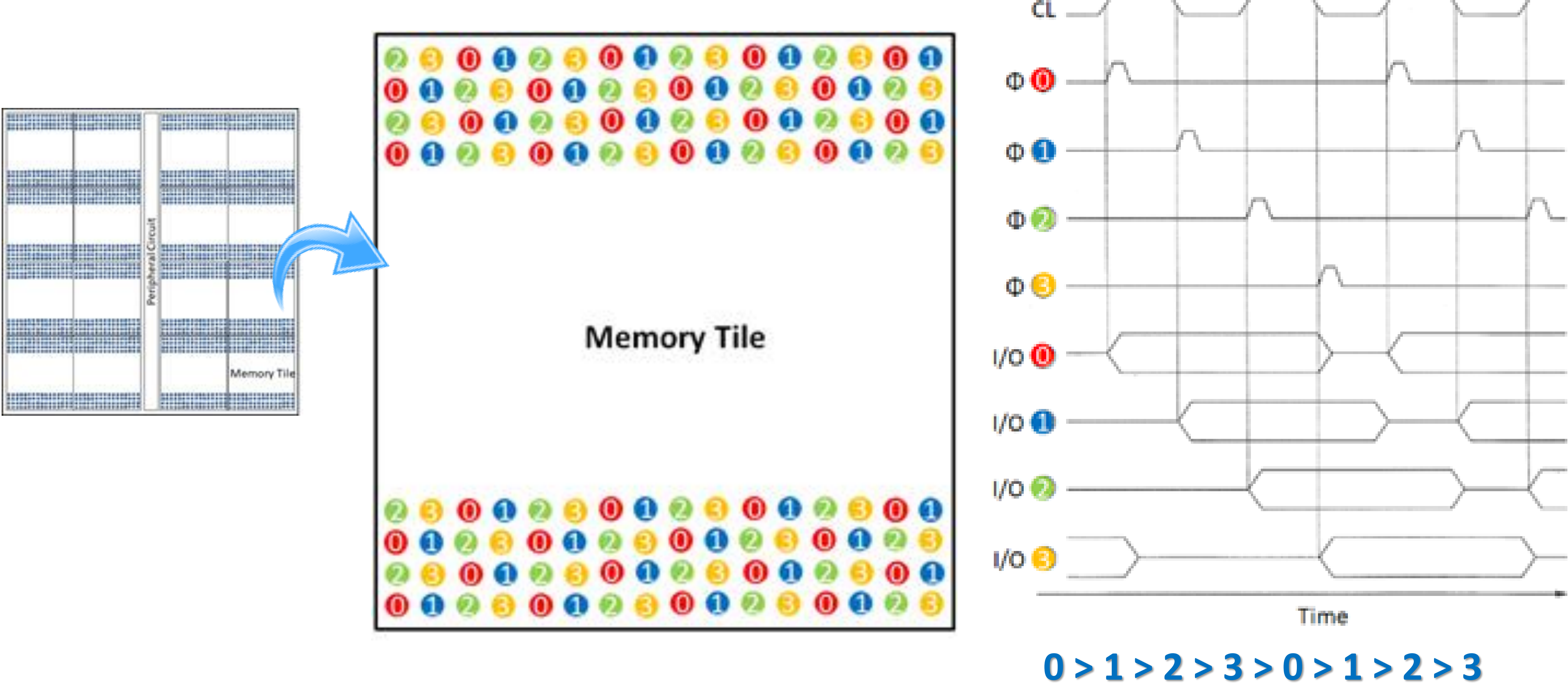
1. K. Sakui and T. Ohba, "High Speed, Low Power, and Ultra-small Operating Platform with Three-dimensional Integration (3DI) by Bumpless interconnects," in the *IEEE IMW Dig. Tech. Papers*, pp.60-63, May 2019. .
2. K. Sakui and T. Ohba, "High Bandwidth Memory (HBM) and High Bandwidth NAND (HBN) with the Bumpless TSV Technology," in the *IEEE 2019 International 3D Systems Integration Conference Dig. Tech. Papers*, Paper Id: 3DIC2019.4005, Oct 2019.
3. T. Ohba, K. Sakui, S. Sugatani, H. Ryoson, and N. Chujo, "Review of Bumpless Build Cube (BBCube) Using Wafer-o n-Wafer (WOW) and Chip-on-Wafer (COW) for Tera-Scale Three-Dimensional Integration (3DI)," *Electronics 2022*, 11(2), doi:10.3390/electronics11020236, pp.1-52, 2022.

Four 3D NAND chips connected through Vertical BL



T. Ohba, K. Sakui, S. Sugatani, H. Ryoson, and N. Chujo, "Review of Bumpless Build Cube (BBCube) Using Wafer-o n-Wafer (WOW) and Chip-on-Wafer (COW) for Tera-Scale Three-Dimensional Integration (3DI)," *Electronics 2022*, 11(2), doi:10.3390/electronics11020236, pp.1-52, 2022.

Parallelism is enhanced, while clock frequency is lowered!



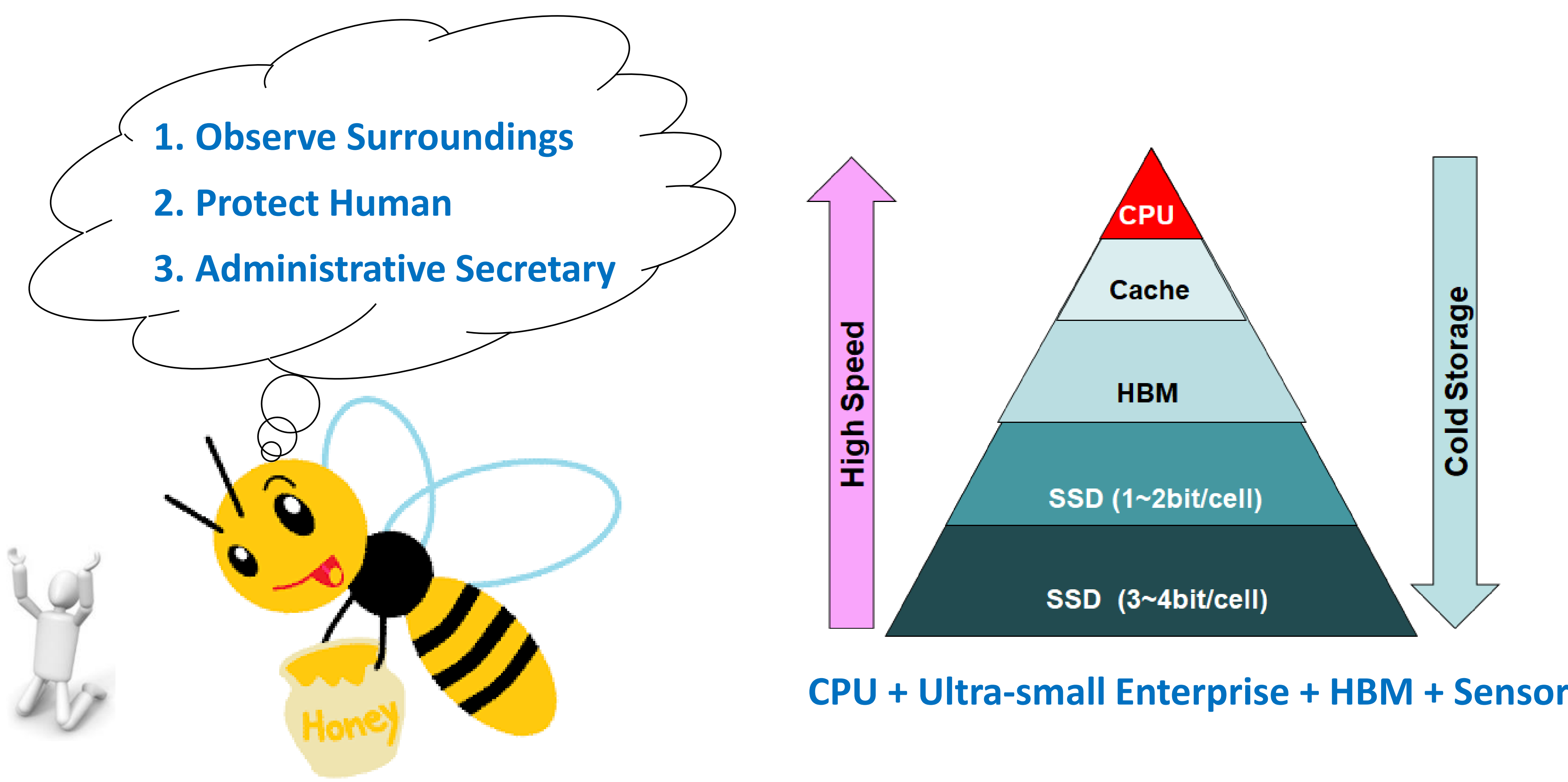
1. K. Sakui and T. Ohba, "Sophisticated Architecture for High Bandwidth Memory (HBM) and High Bandwidth NAND (HBN) with the Bumpless TSV Technology," in the *29th Materials for Advanced Metallization Conference Dig. Tech.* Papers, Nov. 2020
2. T. Ohba, K. Sakui, S. Sugatani, H. Ryoson, and N. Chujo, "Review of Bumpless Build Cube (BBCube) Using Wafer-o n-Wafer (WOW) and Chip-on-Wafer (COW) for Tera-Scale Three-Dimensional Integration (3DI)," *Electronics 2022*, 11(2), doi:10.3390/electronics11020236, pp.1-52, 2022.

BBCube Conclusion

- We proposed a heterogeneous 3DI technology called BBCube 3D
  - Combined use of bumpless WoW and CoW processes with high-density and low-capacitance TSVs
- Two design policies were introduced for low power consumption
  - High parallelism
    - 16k I/Os using 800 Mb/s data rate
  - 3D placement
    - Banks of DRAM are arranged on two dies
    - xPU and cache are divided and stacked
- BBCube 3D achieves
  - 30X higher bandwidth, 20X lower access energy than DDR5
  - 4X higher bandwidth, 5X lower access energy than HBM2E

1. N. Chujo, H. Ryoson, K. Sakui, S. Sugatani, T. Nakamura, and T. Ohba, "Electrical and Thermal Analysis of Bumpless Build Cube 3D Using Wafer-on-Wafer and Chip-on-Wafer for Near Memory Computing," in *Proc. ECTC*, pp.772-777, May 2023.
2. N. Chujo, K. Sakui, S. Sugatani, H. Ryoson, T. Nakamura, and T. Ohba, "Bumpless Build Cube (BBCube) 3D: Heterogeneous 3D Integration Using WoW and CoW to Provide TB/s Bandwidth with Lowest Bit Access Energy," in *Symposium on VLSI Technology and Circuits Digest of Technical Papers*, JFS4-4, pp.1-2, Jun. 2023.

Human Assistant in Mobile

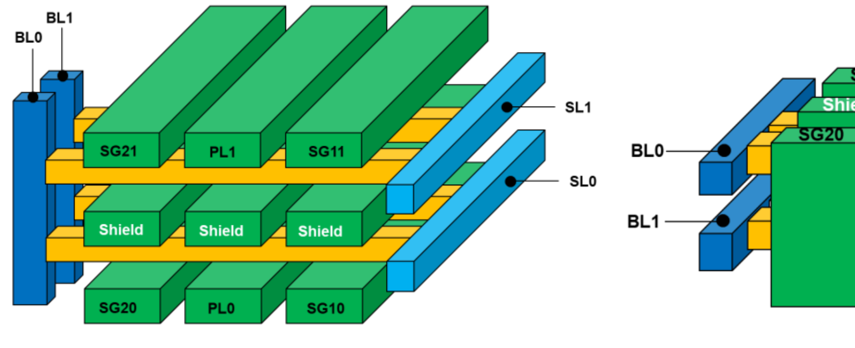


AI Robotic Bee (50mm³, 0.5mW)

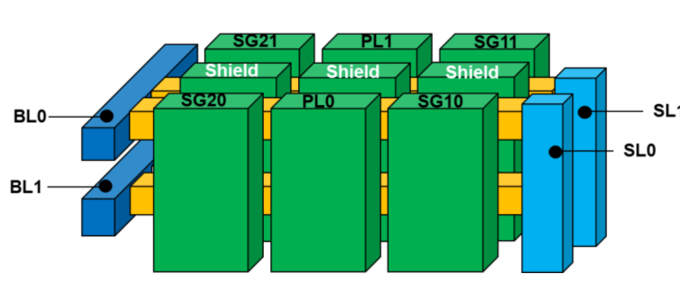
1. K. Sakui and T. Ohba, "Three-dimensional Integration (3DI) with Bumpless Interconnects for Tera-scale Generation," in *the IEEE CICC Dig. Tech. Papers*, 22-6, April 2019.
2. K. Sakui and T. Ohba, "High Speed, Low Power, and Ultra-small Operating Platform with Three-dimensional Integration (3DI) by Bumpless interconnects," in *the IEEE IMW Dig. Tech. Papers*, pp.60-63, May 2019.
3. K. Sakui and T. Ohba, "High Bandwidth Memory (HBM) and High Bandwidth NAND (HBN) with the Bumpless TSV Technology," in *the IEEE 2019 International 3D Systems Integration Conference Dig. Tech. Papers*, Paper Id: 3DIC2019.4005, Oct 2019.

DFM references presented by Unisantis Electronics Singapore

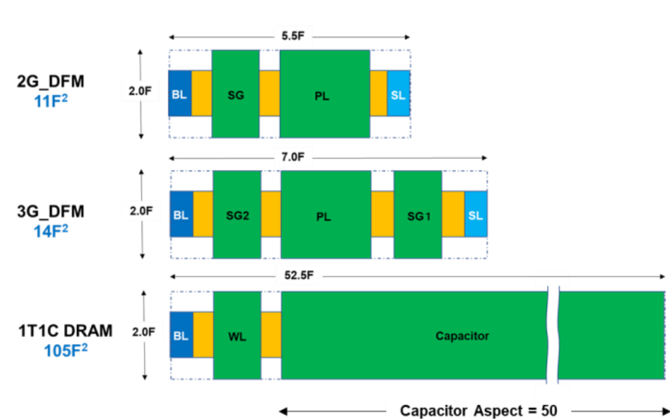
1. K. Sakui and N. Harada, "Dynamic Flash Memory with Dual Gate Surrounding Gate Transistor (SGT)," in *Proc. IEEE IMW*, pp.72-75, May 2021.
2. K. Sakui and N. Harada, "Dynamic Flash Memory with Dual Gate Surrounding Gate Transistor (SGT) for Computation In Memory," in *SSDM*, B-5-06, pp.127-128, Sep. 2021.
3. K. Sakui and N. Harada, "Dynamic Flash Memory with Fast Block Refresh feature using Double Storage Gates and One Select Gate," in Memories - Materials, Devices, Circuits and Systems, Elsevier, 2, 1000007, pp.1-5, Jul. 2022.
4. K. Sakui, M. Kakumu, and Nozomu Harada, "Perfect Read Non-Destructive Dynamic Flash Memory (DFM)," *2022 Flash Memory Summit*, OMEM-301-2, Aug. 2022.
5. K. Sakui and N. Harada, "Read Non-Destructive Dynamic Flash Memory (DFM) with Dual and Double Gates," in *SSDM*, F-4-02, pp.405-406, Sep. 2022.
6. K. Sakui, M. Kakumu and N. Harada, "Dynamic Flash Memory with Fast Block Refresh," in *NVMTS (Non-Volatile Memory Technology Symposium)*, pp.15-16, Dec. 8, 2022.
7. K. Sakui, Y. Li, M. Kakumu, K. Kanazawa, I. Kunishima, Y. Iwata, and N. Harada, "Design Impact on Three Gate Dynamic Flash Memory (3G_DFM) for Long Hole Retention Time and Robust Disturbance Shield," in *Memories - Materials, Devices, Circuits and Systems*, Elsevier, 4, 100054, pp.1-5, May 2023.
8. M. Kakumu, Y. Li, K. Sakui, and N. Harada, "Fully bulk CMOS compatible Key Shape Floating Body Memory (KFBM)," in *Memories - Materials, Devices, Circuits and Systems, Elsevier*, 4, 100061, pp.1-5, May 2023.
9. K. Sakui, Yisuo Li, Masakazu Kakumu, and N. Harada, "Three Gate Dynamic Flash Memory (3G_DFM)," in *ICLED-2023*, IV4, p.50, Jul. 2023.
10. K. Sakui, Yisuo Li, M. Kakumu, and Nozomu Harada, "Stacked Dynamic Flash Memory (DFM) for a High Density Memory," *2023 Flash Memory Summit*, OMEM-202-1, Aug. 2023.
11. K. Sakui, Yisuo Li, Yoshihisa Iwata, Masakazu Kakumu, and N. Harada, "2 bit/cell Dynamic Flash Memory with Three Gates," in *SSDM*, FS-2-22, pp.695-696, Sep. 2023.
12. K. Sakui, "High-Density and High-Performance Technologies for Future Memory," *2023 IEDM Short Course 2*, Dec. 2023.



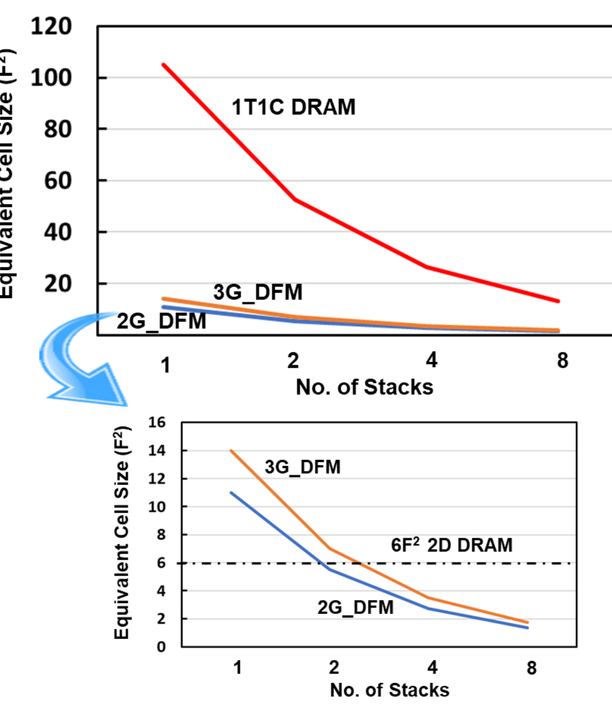
Two Stack DFM (Horizontal Gate)



Two Stack DFM (Vertical Gate)



Equivalent Cell Size



BBCube references presented by Tokyo Institute of Technology

1. K. Sakui and T. Ohba, “Three-dimensional Integration (3DI) with Bumpless Interconnects for Tera-scale Generation,” in *the IEEE CICC Dig. Tech. Papers*, 22-6, April 2019.
2. K. Sakui and T. Ohba, “High Speed, Low Power, and Ultra-small Operating Platform with Three-dimensional Integration (3DI) by Bumpless interconnects,” in *the IEEE IMW Dig. Tech. Papers*, pp.60-63, May 2019.
3. K. Sakui and T. Ohba, “High Bandwidth Memory (HBM) and High Bandwidth NAND (HBN) with the Bumpless TSV Technology,” in *the IEEE 2019 International 3D Systems Integration Conference Dig. Tech. Papers*, Paper Id: 3DIC2019.4005, Oct 2019.
4. N. Chujo, K. Sakui, H. Ryoson, S. Sugatani, T. Nakamura, and T. Ohba, “Bumpless Build Cube (BBCube): High-Parallelism, High-Heat-Dissipation and Low-Power Stacked Memory Using Wafer-Level 3D Integration Process,” in *2020 Symp. on VLSI Technology Dig.*, Jun. 2020.
5. S. Sugatani, N. Chujo, K. Sakui, H. Ryoson, T. Nakamura, and T. Ohba, “Bumpless Build Cube (BBCube) using Wafer-on-Wafer (WOW) Technology with 3D-manner Redundancy Scheme,” in *2020 SSDM Dig.* C-4-03, Sep. 2020.
6. K. Sakui and T. Ohba, “Sophisticated Architecture for High Bandwidth Memory (HBM) and High Bandwidth NAND (HBN) with the Bumpless TSV Technology,” in *the 29th Materials for Advanced Metallization Conference Dig. Tech. Papers*, Nov. 2020.
7. S. Sugatani, N. Chujo, K. Sakui, H. Ryoson, T. Nakamura, and T. Ohba, “Vertically Replaceable Memory Block Architecture for stacked DRAM Systems by Wafer-on-Wafer (WOW) Technology,” *IEEE Trans. Electron Devices*, Vol.67, No.11, pp. 4606-4610, Nov. 2020.
8. S. Sugatani, N. Chujo, K. Sakui, H. Ryoson, T. Nakamura, and T. Ohba, “Vertically Replaceable Memory Block Architecture for Stacked DRAM Systems by Wafer-on-Wafer (WOW) Technology,” *IEEE ESSDERC/ESSCIRC 2021*, B1L-6, Sep. 2021.
9. Z. Chen, N. Araki, Y. Kim, T. Fukuda, K. Sakui, T. Nakamura, T. Kobayashi, T. Obara, and T. Ohba, “Ultra-Thinning of 20 nm-Node DRAMs down to 3 µm for Wafer-on-Wafer (WOW) Applications,“ *IEEE 71st Electronic Components and Technology Conference (ECTC)*, pp. 1131-1137, 2021.
10. T. Ohba, K. Sakui, S. Sugatani, H. Ryoson, and N. Chujo, “Review of Bumpless Build Cube (BBCube) Using Wafer-o n-Wafer (WOW) and Chip-on-Wafer (COW) for Tera-Scale Three-Dimensional Integration (3DI),” *Electronics 2022*, 11(2), doi:10.3390/electronics11020236, pp.1-52, 2022,
11. N. Chujo, H. Ryoson, K. Sakui, S. Sugatani, T. Nakamura, and T. Ohba, “Electrical and Thermal Analysis of Bumpless Build Cube 3D Using Wafer-on-Wafer and Chip-on-Wafer for Near Memory Computing,” in *Proc. ECTC*, pp.772-777, May 2023.
12. N. Chujo, K. Sakui, S. Sugatani, H. Ryoson, T. Nakamura, and T. Ohba, “Bumpless Build Cube (BBCube) 3D: Heterogeneous 3D Integration Using WoW and CoW to Provide TB/s Bandwidth with Lowest Bit Access Energy,” in *Symposium on VLSI Technology and Circuits Digest of Technical Papers*, JFS4-4, pp.1-2, Jun. 2023.